**Dual T1 Card** 

**Version 3.1** 

RELEASE NOTES

## About these Notes

These notes cover new features available in the Dual T1 Card as of Release 3.1.1. The major feature offered in this Total Control product release is TDM clock sourcing when a T1 and PRI card coexist in the same chassis.

The revision number of the firmware can be identified by accessing the T1 card's command line configuration program through your terminal emulator:

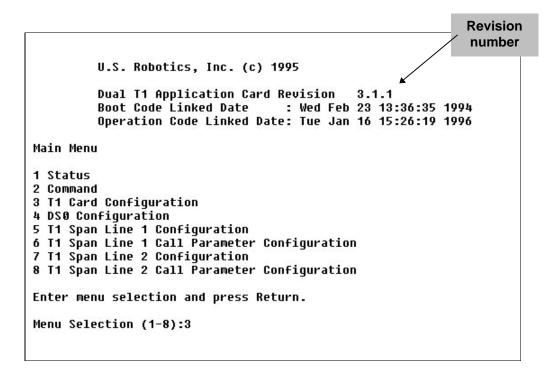


Figure 1. T1 Card Command Line Configuration Screen

The configuration parameters affected by release 3.1.1 can be located in Menu Selection 3, T1 Card Configuration.

## T1 and PRI Timing Source Relationship

Timing on the TDM bus is critical when delivering accurate, properly multiplexed data to digital modems for conversion. Since both T1 and PRI cards access the TDM bus for clock reference, a timing source must be established that accommodates both. When an individual T1 card is installed in the Total Control chassis, the setting of timing source priorities (shown in figures 2 and 3) remains as in previous releases. The scenario changes, however, when PRI cards are introduced to the chassis.

```
T1 Card Configuration
                                                Current Setting
1 Save current Configuration to NVRAM
2 Restore NVRAM Configuration
3 Restore Default Configuration
4 Timing Source Priority Assignment
                                              T1-1=1 T1-2=2 INT=0
(NOTE: If this T1 card is in the slave mode, it will use
       the TDM clock and ignore the clock switching task.)
(NOTE: Changing configuration parameters may affect calls in progress.)
Enter menu selection and press Return or press Esc to exit.
Menu Selection (1-4):
```

Figure 2. T1 Card Configuration Screen

```
Timing Source Priority Assignment
T1 Span Line Line 1 (T1-1): 1
T1 Span Line Line 2 (T1-2): 2
Internal Clock (INT): 0
Enter the desired priority (0-3) beneath each timing source and
press Return or press Esc to exit.
0 = Disabled, 1 = Highest Priority, 3 = Lowest Priority
Timing Source Priority Assignment
Timing Source:
                        T1-1 T1-2 INT
Timing Source Priority:
```

Figure 3. Timing Source Priority Assignment Screen

## T1 "Slave" and PRI "Master"

As ISDN becomes widely accepted and installed, the inclusion of PRI cards into existing and new chassis requires the setting of the timing source on the TDM bus. With both card types in the chassis, the PRI timing priorities take precedence over the T1 card. The T1 card becomes a "slave" to the PRI and all timing on the TDM bus is directly driven from the span 1 or span 2 inputs on the "master" PRI card. As noted in Figure 2, if the T1 card coexists with a PRI card, it will use the TDM bus timing (PRI source) and any priorities reset in option 4 will be ignored.

## T1 and Multiple PRIs

The existence of multiple PRI cards in a chassis will create a default pattern that maintains timing integrity automatically. As depicted in Figure 4 below, the timing source will originate from the PRI card in slot 2. If this card becomes disabled, the card in slot 3 will assume the timing source responsibilities, and so on through slot 5. If the final PRI is disabled, the timing source will default to the T1 card in slot 1. The default scenario remains the same no matter how many PRI cards you are employing (up to 4).

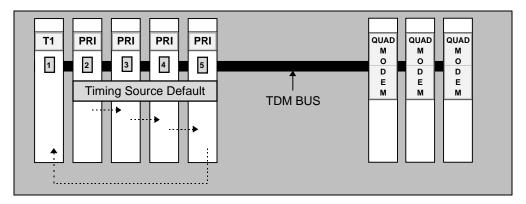


Figure 4. Multiple PRI Timing Source Default Pattern

Even though the timing on the TDM bus is driven from the PRI span lines, the T1 cards timing sources priorities should be set to accommodate the continuation of T1 service should the existing PRI card(s) become disabled. Should the PRI card become non-functional, the T1 card will reboot and default to its own timing source priorities. Typically, the default settings will accommodate this provision.

Finally, the T1 card will require 2 minutes to boot to allow for the establishment of the timing source from the PRI card. This will not affect the performance of the card once this boot period is over, but do not access or remove the card during this process.

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