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Go into any circuit design lab and on just about every bench you'll find an oscilloscope, its glowing blue or green eye displaying one or a group of waveforms that the owner of the bench considers important. Designers spend hours staring at these fluorescent eyes, fine tuning their circuits until those waveforms look exactly the way they should. The oscilloscope's ability to display repetitive waveforms makes it a ubiquitous and essential instrument not only in the R&D lab, but also in the service engineer's tool kit and in production test areas, where it's been something of an anomaly. Often the oscilloscope is the only instrument in an automated production test system that has to be set up manually and can't talk to the computer.

Now that can change. Our cover subject this month is an oscilloscope measurement system that can set itself up automatically or at the direction of a computer. The 1980A/B (it comes in a low, wide B model and a taller A model) can talk to the computer over the HP Interface Bus, HP's version of an industry standard communication method for programmable instruments. This programmable scope can capture and display a signal without any knob-twisting by the operator—that's called Autoscope. With its digital waveform storage option, it can take, store, and display samples of a waveform, transmit those samples to a computer, and get samples back for display along with messages for the operator. Another option, a plot/sequence memory, lets the operator initiate a predefined sequence of measurements by pushing a single button on a probe.

You'll find the story of the 1980A/B design on pages 3 to 26. Our cover photo shows a 1980B talking to an HP 9826A Computer in a lab bench test setup at Fairchild Camera and Instrument Corporation in Mountain View, California. Our thanks to Fairchild for their cooperation.

In the world of microwave frequency sources, the big three are signal generators, sweep oscillators, and synthesizers. Synthesizers offer the ultimate in frequency accuracy and stability and are generally more expensive than the others. The article on page 30 describes a new instrument, Model 5344S Source Synchronizer, that gives sweepers and signal generators the accuracy of a synthesizer, turns signal generators into sweepers, at least for narrowband sweeps, and greatly improves the accuracy of a sweep oscillator's wide sweeps by means of a procedure called "lock and roll." For much less than the cost of a synthesizer, the owner of a sweeper or signal generator can have synthesizer accuracy, some new capabilities, and a general-purpose microwave counter (part of the 5344S). It's like getting the best of two worlds for the cost of one and a half.

Many HP products contain proprietary HP integrated circuits as well as commercially available ICs. A variety of processes are used to produce these HP ICs. The article on page 27 describes one such process, a new high-performance bipolar process being developed by HP's Integrated Circuits Division in Santa Clara, California. Other processes will be described in upcoming issues.

-R. P. Dolan

Oscilloscope Measurement System Is Programmable and Autoranging

This new concept in oscilloscopes is a significant aid to measurement productivity.

by William B. Risley

IN THE DESIGN, manufacture, and service of electronic equipment no other instrument is so ubiquitous as the oscilloscope. Early in the technical curricula, students are introduced to the analysis of time-variant phenomena. The display of signal amplitude as a function of time provided by an oscilloscope has become firmly established in electrical engineering because of its ability to provide a faithful reproduction of the electrical activity at a given circuit node. So important is this method of analysis that oscilloscopes have come to accommodate a wide range of signal types. Signals may vary by five orders of magnitude in amplitude and by nine orders of magnitude in duration and still be meaningfully analyzed with a single instrument. Because of their range of application, oscilloscopes have become complex instruments, able to move facilely from one situation to another.

The thrust of today's measurement trends is towards higher levels of automation and the increased use of data bases. Most oscilloscopes, however, are not computer-controllable or systems compatible. Hewlett-Packard's response to this lack is a new breed of oscilloscope, Model 1980A/B Oscilloscope Measurement System, Fig. 1.

Computer Architecture

The 1980A/B Oscillosope Measurement System is an automated HP-IB*-compatible instrument that makes significant contributions to the viewing, measuring, and processing of time-domain waveforms. With its microprocessor-based computer architecture, the 1980A/B is a multifunction, multifaceted instrument. Internally, it is divided into eight functional blocks that interface with each other by means of a bus structure (Fig. 2). This extensive digital control permits such features as an easy-to-use front panel, autoranging, complete programmability, digital waveform storage, and hardware and firmware expandability. Unlike other oscilloscopes, the 1980A/B's innovative front panel has a single rotary control. Color-coded touch keys arranged in a logical hierarchy are used for setting up

*HP-IB is Hewlett-Packard's implementation of IEEE Standard 488 (1978).

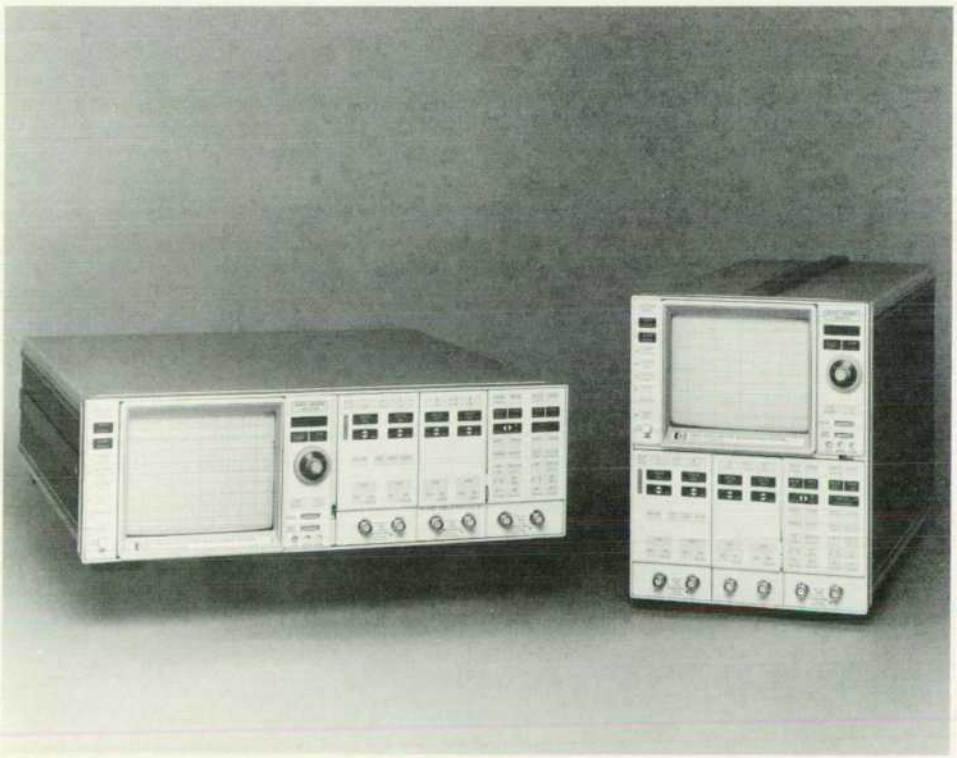

Fig. 1. *Designed for use in automated systems, Model 1980A/B Oscilloscope Measurement System is compatible with the HP-IB (IEEE 488). Among its features are Autoscope, which gives the user a display rapidly and automatically, and front-panel calibration. Options include digital waveform storage and measurement sequence memory. (r) Model 1980A. (l) Model 1980B.*

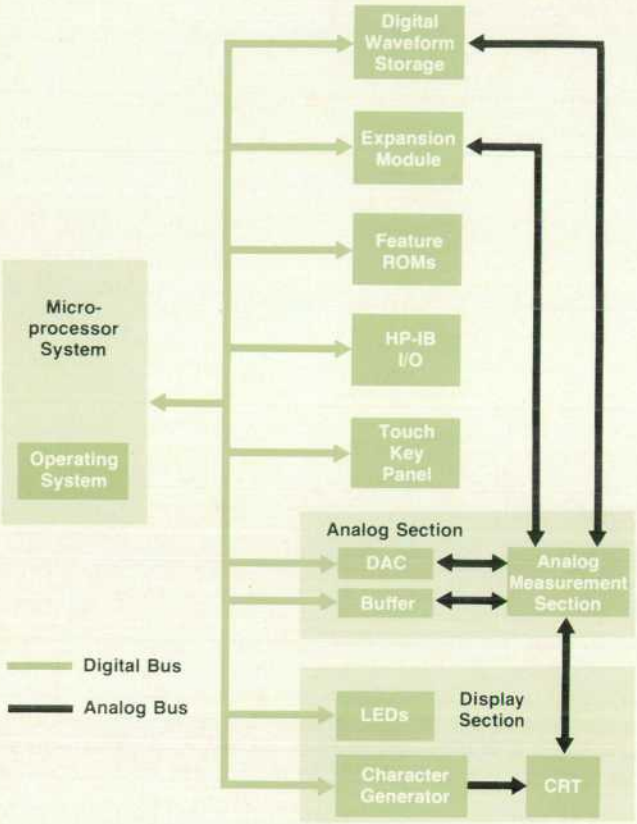

Fig. 2. *Simplified 1980A/B architecture.*

the instrument, while the rotary control is used to adjust variable functions.

The display section permits the operator to interact with the instrument through the CRT, which displays both real-time and digitally stored waveforms, scale factors, and advisory messages. The display section includes an option menu, softkeys, eight nonvolatile save/recall registers, and intensity controls. Standard option menus include automatic instrument preset, front-panel calibration, automatic delay and input amplifier balancing, confidence tests to verify operation, and front-panel setting of the HP-IB address and operating modes. Menus are automatically updated as hardware and firmware are added.

When an invalid operation is attempted, advisory messages are momentarily displayed on the CRT. Invalid measurements are impossible using the 1980A/B, and the advisory messages help the operator use the instrument to its capacity. Error codes, displayed on light-emitting-diode (LED) lamps, provide information about internal malfunctions.

In its basic configuration, the 1980A/B offers two 100-MHz analog measurement channels with 2-mV/div deflection factors, two independent and direct 5-ns/div sweeps, main or delayed trigger view, delta-time and delta-voltage measurements, and a multitude of automated features including Autoscope, which allows the user to obtain a display rapidly without adjusting individual controls, and front-panel calibration, which lets the user calibrate the instrument in about 25 minutes by following instructions displayed on the CRT.[1]

Feature ROMs can be added to expand resident programmed firmware measurement capabilities. For example, an optional Plot/Sequence ROM, Model 19811A, lets the user program as many as 25 front-panel keystrokes for each front-panel input; each stored key sequence can later be activated using a probe pushbutton.

Remotely programmed operation is provided through a standard HP-IB port that interfaces with all functional blocks through the internal bus. All measurement parameters can be programmed, and touch key operation, CRT instruction display, and installed-enhancements addressing are also programmable. Touch key status, measurement results, and digitally stored waveforms may be sent to a computer/controller for processing.

With the HP-IB interface, the 1980A/B can be combined with other HP-IB-compatible instruments to form a completely automated test system. Because the 1980A/B is fully programmable, test routines can be established, stored, and used repeatedly.

With the addition of a 19860A Digital Waveform Storage Option (see article, page 15), the 1980A/B can be used as a complete test system for time-domain measurements. With the 19860A installed, repetitive events to 100 MHz or single-shot events to 5 kHz can be captured, displayed, and sent to a computer via the HP-IB for analysis. This results in complete answers without operator intervention. For example, a series of standard signals may be digitized and stored in a computer as a reference library for automatic testing. As tests are performed, signals may be automatically compared in software.

Summary

The 1980A/B is a timely response to today's economic, measurement, and technological trends. The concept of combining a broad range of oscilloscope capabilities, full programmability, and digital waveform storage into a highly flexible, interactive measurement system provides a new tool for computer-aided applications. This instrument is now at work in many systems in design, engineering, and production test.

Reference

1. P. Austgen, W. Watry, and M. Karin, "Software-based design automates scope operations," Electronics, March 10, 1981, pp. 181-188.

William B. Risley

Currently oscilloscope R&D manager of HP's Colorado Springs Division, Bill Risley was project and section manager for the 1980A/B. He joined HP's oscilloscope lab in 1972 as a design engineer on the 1722A Oscilloscope. He holds an MSEE degree from Colorado State University and a BA degree in physics from Princeton University. Away from HP, Bill keeps busy with his family—he has two sons—church activities, and gardening and foresting on his twenty acres in Black Forest, Colorado.

Designing the Oscilloscope Measurement System

by Russell J. Harding, Monte R. Campbell, William E. Watry, John R. Wilson, and Wilhelm Taylor

IN THE 1980A/B Oscilloscope Measurement System, the microprocessor brings the added dimension of programmability to the oscilloscope, making automatic waveform measurements possible. Rise time, voltage, width, and delay measurements and event detection can be attained through firmware and software.

The architecture of the 1980A/B is shown in Fig. 1. The hardware consists of a digital control section, an analog measurement and display section, and the interfaces between these sections.

The digital control section is based on the 8085 microprocessor and associated chip set. The 8257 programmable DMA controller and the 8275 programmable CRT controller chips generate characters for the CRT readout. The 8355 I/O ROMs control switch functions such as range selections and channel on/off. The 8155 timer is used by various elements of the firmware, such as the control knob section, to time events. The HP-IB* section uses the 8291 HP-IB talker/listener chip, which is tied to the 8085 bus. The expansion module is also tied to the 8085 bus.

Fig. 2 shows the fixed allocation of the possible 64K bytes of addressable memory locations in the firmware operating system. The firmware that controls the basic 1980A/B system is contained in the lower 32K of available address space, while the upper address space is dedicated to system expansion. All feature ROMs and options can call upon utilities and subroutines that reside in the main operating system.

All oscilloscopes contain vertical, horizontal, trigger, and display systems. In the 1980A/B, these are in the analog section. Because the 1980A/B is microprocessor-controlled, the horizontal, vertical, and trigger systems are programmable and are designed to make full use of the microprocessor. This requires that these systems be somewhat different from their conventional, nonprogrammable predecessors.

The 1980A/B's digital and analog sections are coupled through serial latch packs, a horizontal hybrid interface, a 16-channel custom DAC (digital-to-analog converter), and a custom DAC refresh controller. Hewlett-Packard designed the DAC refresh controller IC to provide the DAC with a continuous update of state information. DAC numbers between 0 and 2999 are sequentially fetched from 16 fixed locations in memory and serially transferred to the DAC by the DAC refresh controller independently of the 8085 processor. The DAC then translates the numbers to analog voltages, which control analog functions such as sensitivity, position, and trigger levels. The DAC hybrid also serves as the decoder for the LED displays.

*HP-IB is Hewlett-Packard's implementation of IEEE standard 488 (1978).

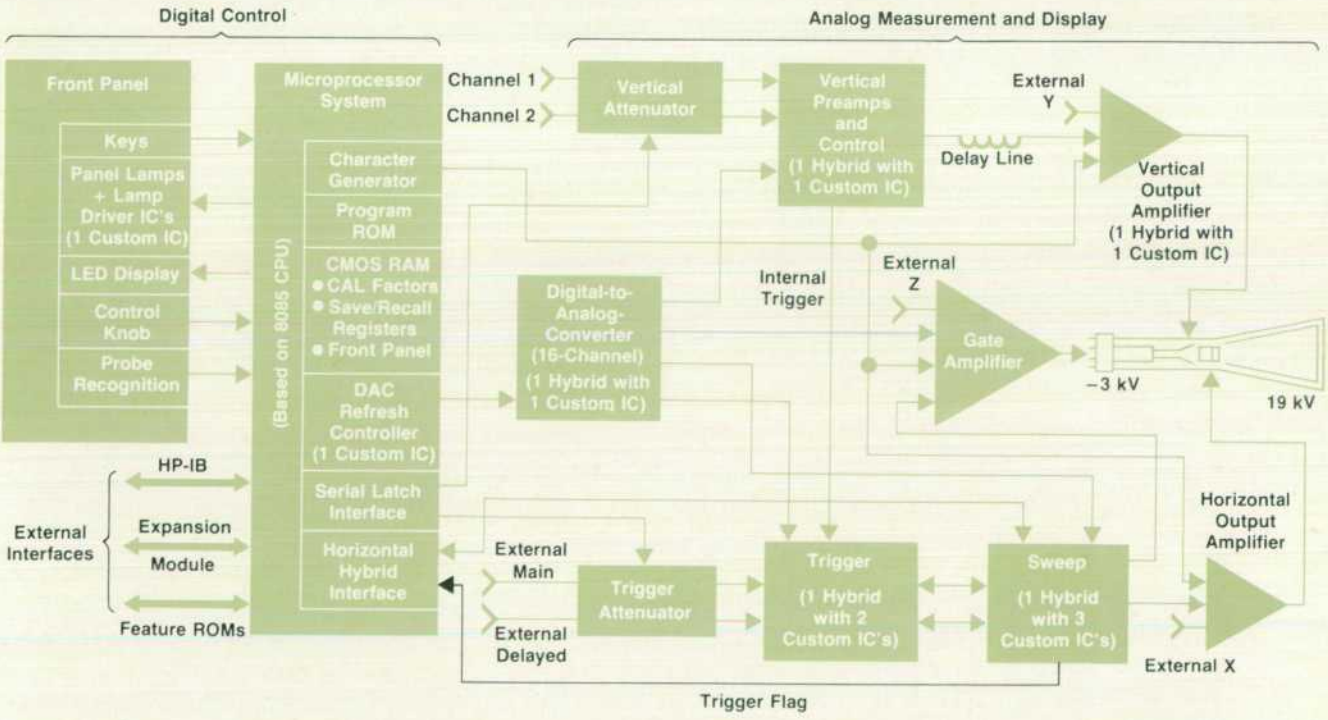

Fig. 1. *1980A/B Oscilloscope Measurement System simplified block diagram.*

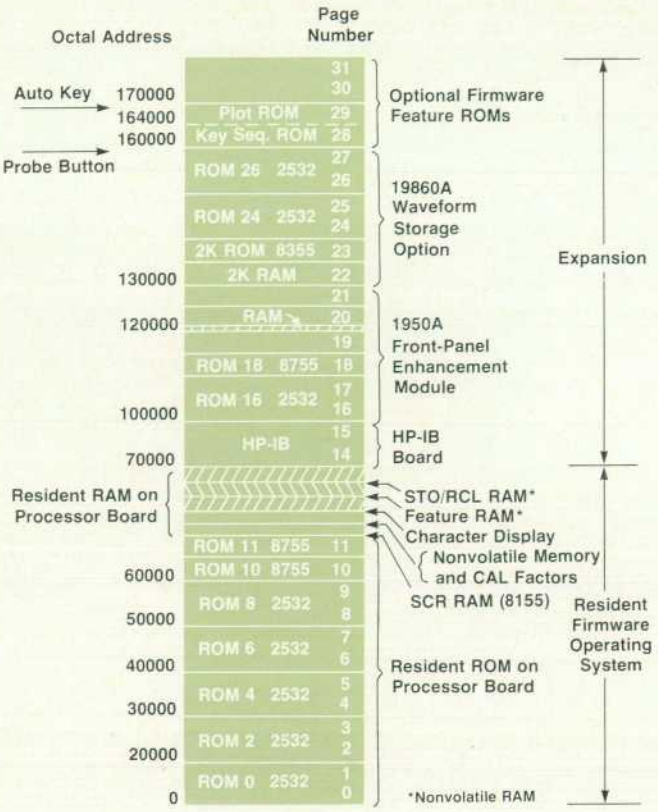

Fig. 2. *1980A/B memory allocation.*

Adapting the Analog Section

As the first step in making a programmable oscilloscope measurement system, the functions switched or controlled mechanically from the front panel of a conventional oscilloscope had to be electronically switched or controlled so that the microprocessor could control these functions. In the 1980A/B, the microprocessor has three ways of controlling the instrument: two are by switching and the other is analog. One of the switching sources originates in the microprocessor control system, and a 56-bit serial data bus distributes it throughout the instrument. The serial data bus is made up of latching shift and store registers that interface the bus to the various microprocessor-controlled circuits. The second switching control source originates in the horizontal section of the 1980A/B and controls functions that have to be switched in real time (e.g., channel selection for alternate or chop display modes). The third source, the microprocessor-controlled DAC, controls analog functions such as vertical position.

Horizontal System

An oscilloscope's horizontal system, which functions as a time scaler, generates main and delayed sweeps, delay time, and the associated control signals needed for viewing a range of time bases. In conventional oscilloscopes, these functions are restricted by the delay time generator, and delay time is achieved with an analog comparator. One input of this comparator is the main ramp voltage, and a variable resistor attached to the front-panel delay control knob controls the other input. As the main ramp voltage changes, causing the CRT beam to move across the screen, the delayed sweep is enabled by the comparator. The delayed sweep begins immediately if the delayed sweep is in auto mode, or at the next delayed trigger if the delayed sweep is in the trigger mode. Delay times are varied by varying the comparator voltage. Since delayed sweeps are used to expand sections of the main sweep, they must sweep faster than the main sweep. Delayed sweeps are normally terminated at the end of the main sweep if not already completed.

The 1980A/B's horizontal system differs from those in conventional oscilloscopes in that its delay time generator is programmable and the main and delayed sweeps are independent. These two differences effectively eliminate the restrictions found in conventional horizontal systems, and they are possible because of the structure of the horizontal system and how it interacts with the microprocessor. Delay times from 0 to 9.9999999999 seconds can be programmed via the HP-IB or from the front panel, and both main and delayed sweeps can be independently programmed from 5 ns/div to 1 s/div. With the 1980A/B, delay times are no longer dependent on the main sweep, and delayed sweep speeds are no longer restricted by main sweep speeds.

The advantages realized from this independent control become apparent while operating the 1980A/B manually. For example, it is possible to change the main sweep to achieve a more convenient display and not affect the delay time or delay sweep speed. This is particularly helpful when viewing both main and delayed sweeps in the dual mode.

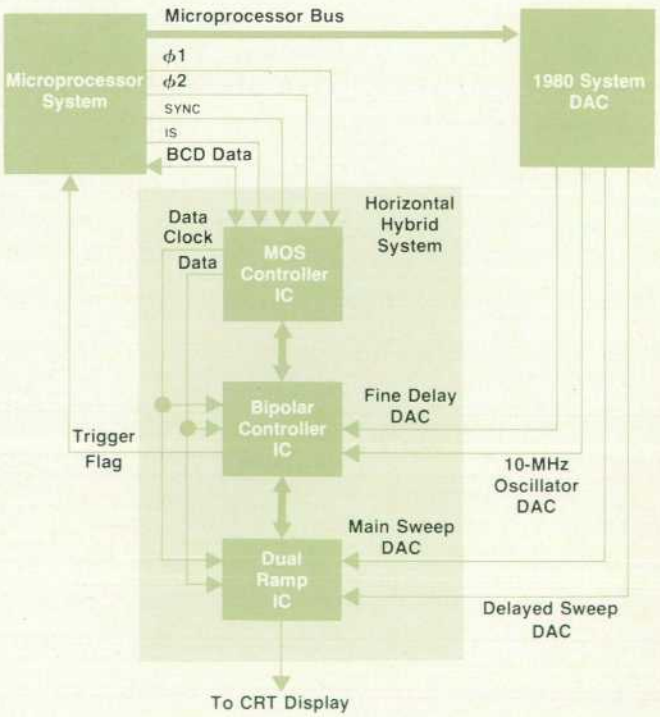

Fig. 3. *The 1980A/B horizontal hybrid system. The system DAC has 16 channels. Four of these are used by the horizontal system.*

The absence of interaction between display functions simplifies not only manual control but also HP-IB control. Measurements over the HP-IB can be made using a one-bit flag that looks for trigger events during programmed time windows. This is called the trigger flag. Time windows for the trigger flag are established by the delayed sweep gate, which is at a higher logic level while the delayed ramp is running. Therefore, the width of the time window is determined by the delayed sweep speed, and the start of the time window is set by the delay time. These are independent parameters.

The heart of the 1980A/B's horizontal system is the horizontal hybrid circuit. Three custom integrated circuits—the dual ramp IC, the bipolar controller IC, and the MOS controller IC—and an assortment of resistors and capacitors are all contained in this thick-film hybrid (Fig. 3). Each IC represents a major functional area.

Independent main and delayed sweeps are generated on the dual ramp IC. The ramp circuitry on this IC is identical for both main and delayed sweeps, and they share a common output buffer and beam blanking logic. Because the main and delayed time bases have the same circuitry and are programmed identically, they perform identically and are truly independent.

Sweep speeds in the 1980A/B are continuously variable, unlike the traditional 1, 2, 5 sequence of discrete settings (e.g., 1 μs/div, 2 μs/div, 5 μs/div). Sweep ramp voltages are generated by charging a fixed capacitor with a constant-current source. In the 1980A/B, the size of this capacitor is digitally programmed while the current source is controlled by the 1980A/B's system DAC. Capacitor size establishes the exponent of the sweep speed and the system DAC determines the mantissa. For example, to set a sweep speed of 6.23 μs/div, the capacitor size is programmed for the 1.0-μs-to-9.99-μs range. Then the DAC voltage, which controls the current sources, is programmed to establish the proper current. Using this method, sweep speeds are always calibrated, even at 6.23 μs/div.

Custom Microcircuits Make the 1980A/B Possible

The 1980A/B Oscilloscope Measurement System mainframe uses 17 custom monolithic ICs distributed among five custom hybrid circuits and six packaged parts. The technologies employed include a high-frequency process, a high-density bipolar LSI process, an N-channel MOS process, and both thin-film and thick-film hybrid processes.

The high-frequency process is a shallow planar process which produces transistors with typical cutoff frequencies (f_T) of 2.2 GHz and subnanosecond switching speeds. Base insert and collector wall diffusions are included to reduce base and collector resistance to achieve the high performance. Tight alignment tolerances and 2.5-μm minimum features provide small devices but comparatively limited complexities.

The LSI process is similar but has a higher level of complexity. This process has a thicker epitaxial layer and deeper base and emitter diffusions, but eliminates the base insert and collector wall diffusions, and so has fewer masking operations and relaxed design rules. Typical LSI transistor cutoff frequencies are about 1 GHz, resulting in switching speeds and propagation delays of about 1 ns.

Other custom microcircuit technologies used include a thin-film tantalum-nitride resistor network in the digital-to-analog converter (DAC) hybrid and several high-density N-channel MOS ICs used in both the DAC and horizontal hybrids to implement the control logic functions.

Thick-film hybrid technology is used to interface the various custom ICs with commercially available ICs and precision resistors and capacitors. The circuitry is partitioned into four major hybrids (see Fig. 1): the DAC, the vertical preamplifier, the trigger circuit, and the horizontal system. Using thick-film hybrids and custom ICs, the circuit density of the 1980A/B is at least an order of magnitude greater than an equivalent printed circuit board implementation. Also, a significant high-frequency performance advantage was realized thanks to the small conductor trace widths, the laser-trimmed 1% resistors, and the short trace lengths between adjacent components. Without the performance advantage of the high levels of integration and circuit density achieved, the 1980A/B would not have been a feasible project.

Early in the development program it was clear that manufacturing technologies would have to be improved to achieve cost-effective production of these hybrids. Since each hybrid requires about 90 wire bonds, an automated wire bond process was developed. To achieve consistent, well controlled assembly of the add-on components, an automated hybrid assembly process was developed. A new hybrid test system was designed to facilitate rework. Because most electronic failures are recurrent and computers are extremely efficient at repetitive problems involving memory work, a computer was trained to troubleshoot hybrids by entering known solutions to specific failure modes. The computer compares symptoms of the hybrid under test with the history of all past failures. It then chooses the best cure for the particular failure mode. If no correlation is found, it will request aid from the technical staff. Since there is an on-going interface between the computer and the technical staff, the failure history file is continually updated and a complete record of past failures can be accessed.

-William Duffy
-John Meredith
-Mike McTigue

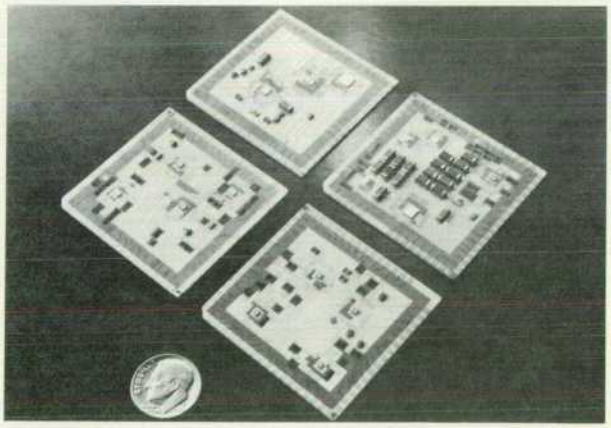

Fig. 1. *The four major hybrids of the 1980A/B. From top, clockwise, the horizontal system, digital-to-analog converter (DAC), trigger circuit, and vertical preamplifier.*

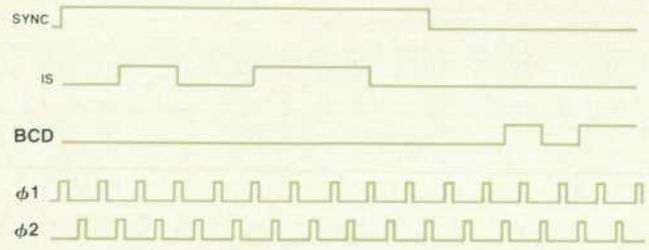

Fig. 4. *The MOS controller IC controls the transfer of data from the microprocessor to the horizontal system. Data is transferred synchronously over three serial data lines—SYNC, IS, and the BCD line—using two external clocks, ϕ1 and ϕ2.*

A startable 10-MHz oscillator, delay timer, and real-time control are on the bipolar controller IC. The startable oscillator generates an accurate 100-ns (10-MHz) delay clock which is synchronized to the main trigger. Establishing the timing of the delay clock and main trigger allows the delay time to be counted digitally, and this decouples the delay time from the main sweep. For delay times less than 100 ns, an independent fine delay ramp and comparator are used. Fine delays are controlled by varying the initial charge on a fixed capacitor. A constant-current source then discharges the capacitor, generating the fine delay times ranging from 0 to 99.9 ns.

Digitally counting delay times rather than using the analog comparator method of conventional oscilloscopes led to two special features of the 1980A/B: digital delay and automatic delay time calibration. The delay trigger clock replaces the 10-MHz startable oscillator when the 1980A/B is in the digital delay mode. The delay trigger clock goes high each time the delay trigger source satisfies the delay trigger conditions (level and slope). Therefore, the delay time is now a function of delay trigger events. This is particularly useful in finding the nth pulse in a data string that is jittering so badly that it cannot be seen.

During automatic delay time calibration, the 10-MHz startable oscillator frequency is matched to the crystal reference that generates the microprocessor clock. The delay counter is cleared and then allowed to count the 10-MHz startable oscillator clock for a given amount of time. The resulting count is transferred to the microprocessor for evaluation. If the count does not match the expected count, then the oscillator frequency is varied, and the entire process repeated. With completely automatic calibration, the 1980A/B can calibrate its delay time whenever requested. This means that the accuracy and stability of the crystal reference can be applied to every measurement.

The third custom IC in the horizontal hybrid is the MOS controller. All communication between the microprocessor and the horizontal system is handled through three serial data lines connecting this IC to the horizontal interface circuitry in the microprocessor system. Scope mode, coarse delay time, and main and delayed sweep ranges are transmitted over these lines. Fine delay and continuous sweep speeds are controlled via the 1980A/B's DAC system. The MOS controller IC becomes involved in real-time control by counting the holdoff time between sweeps and the upper seven BCD digits of delay time or digital delay count.

Programming the Horizontal System

As stated above, one way that the microprocessor communicates with the horizontal system is through the DAC. Four DAC channels to the horizontal system are available. The main sweep rate, delayed sweep rate, 10-MHz oscillator, and fine delay time DAC channels are used to make fine adjustments in the horizontal system.

The basic digital information the microprocessor transfers to the horizontal system is grouped into three major areas: scope mode, sweep mode, and delay time. As stated above, the MOS controller IC controls the transfer of this data between the microprocessor and the horizontal system. Proper management of this data requires both interrupt and noninterrupt data transfers. Data transfers with interrupt reset the horizontal system, transfer data, and then restart the system using the new data. This type of data transfer is required when changing the scope mode or sweep ranges, and in some automatic measurement applications. Noninterrupt data transfers are used for changing delay times. The horizontal system does not recognize data transferred without an interrupt until the current sweep cycle is completed.

The MOS controller IC design takes advantage of the low power dissipation inherent in dynamic MOS circuit designs. The circuit uses two external clocks, ϕ1 and ϕ2. Data is transferred synchronously with these clocks through three serial data lines: SYNC, IS (instruction), and the bidirectional BCD data line. The data transfer timing is illustrated in Fig. 4. During SYNC high, the instruction line data is shifted into an instruction decoder. If no valid instruction is recognized, the horizontal system continues unaffected. When a valid instruction appears, the MOS controller accepts information on the BCD data line. The first instruction sent to the horizontal system defines the type of data transfer that will follow. That is, it says whether the next data transfer will be with interrupt or without interrupt. After the type of data transfer has been established, all subsequent transfers are that type until another instruction to change the type is received.

A third type of data transfer is used when calibrating the delay time generator. The delay time generator is calibrated

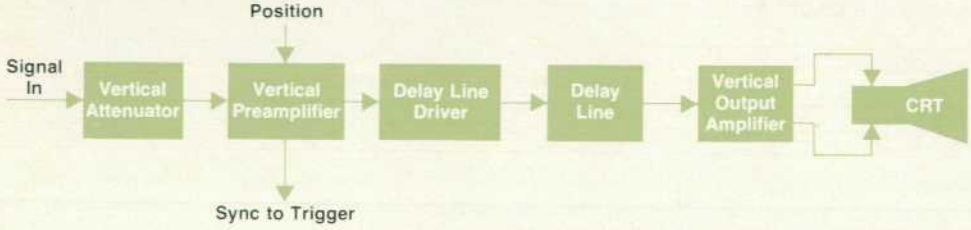

Fig. 5. *1980A/B vertical system block diagram.*

by zeroing the delay counter and then allowing it to run for a predetermined length of time. The upper seven BCD digits of the delay counter are then transferred to the microprocessor via the bidirectional BCD data line. This calibration transfer is the only transfer of data from the MOS controller IC to the microprocessor; all other data transfers go in the other direction. After the microprocessor has received the seven BCD digits, it compares what it received with what it knows should have been received. The difference is used to adjust the frequency of the 10-MHz oscillator. This is repeated until the received data agrees with the expected data. The oscillator's frequency is adjusted by the microprocessor via the 10-MHz oscillator DAC channel. The microprocessor controls the oscillator's frequency by controlling the output voltage, which controls a variable capacitor in the oscillator's LC circuit.

Real-time control of the horizontal system is a coordinated effort between the MOS controller IC and the bipolar controller IC. The bipolar IC receives scope mode data from the microprocessor via the MOS controller IC. Then on a sweep-by-sweep basis, the bipolar IC operates the horizontal system in the appropriate mode. The allowable modes are channel 1 versus channel 2, single sweep, auto or triggered main sweep, auto or triggered delayed sweep, and digital delay. During each sweep cycle the MOS controller IC counts the upper seven digits of the delay time. These digits represent either 1-μs counts or, in the digital delay mode, trigger event counts. Also, at the beginning of each sweep cycle the MOS controller IC counts a 1-MHz clock to establish an appropriate holdoff time as defined in Table I. Holdoff time is required so that the sweep capacitors can discharge completely before a new sweep is started.

The 100-ns digit of the delay time is counted on the control IC. Clocking for this counter is derived from the 10-MHz startable oscillator which is calibrated using the calibration data transfer mentioned earlier. As with the scope mode, the microprocessor sends the 100-ns digit via the MOS controller IC.

Delay time is counted from the most-significant digit to the least-significant digit. For example, delays greater than 1 μs are counted first on the MOS controller IC, which counts in 1-μs steps. After digits 1 μs and greater have been counted, the bipolar IC then counts the 100-ns digits. After all digits have been counted, there remain the delay times ranging from 0 to 99.9 ns. The fine delay circuits on the bipolar IC handle these delays. Fine delay times are set by the DAC. A constant-current source discharges a capacitor to generate the fine delay. The initial voltage on the capacitor is set to the fine delay DAC voltage. Then, at the appropriate time, the capacitor is allowed to discharge to ground, generating an end-of-delay-time signal.

Table I
Holdoff Format
Holdoff time (clock cycles) at 1 MHz

Sweep Speed	Required Holdoff	
	Counts	Time
0.1-1 s	200,000	200 ms
0.01-0.1 s	200,000	200 ms
1-10 ms	2,000	2 ms
0.1-1 ms	2,000	2 ms
0.01-0.1 ms	10	10 μs
1-10 μs	10	10 μs
0.1-1 μs	0	0
0.01-0.1 μs	0	0
5-10 ns	0	0

The microprocessor controls the fine delay by controlling the fine delay DAC output voltage. The fine delay DAC has a range of 0 to +4 volts, representing approximately −25 to +125 ns of delay. The overlap allows for system calibration.

The dual ramp IC also receives data from the microprocessor via the MOS controller IC. Four bits are required by both the main and delay time bases to define their respective sweep ranges completely. Decoding these bits determines the total capacitance and current switched into the ramp circuits. Table II shows the decoding of these bits.

Note that for each total capacitance value two current sources are used, ×1 and ×10. Both current sources are

Allowing for System Expansion

Because of the way in which the microprocessor and oscilloscope are integrated within the 1980A/B Oscilloscope Measurement System, the instrument can handle two separate hardware options and seven firmware features. Hardware options—front-panel expansion modules and a waveform storage card—add only hardware capabilities, but the firmware features are ROMs that can use existing hardware to implement new features or measurement sets. Memory space is allocated for each of these expansion modes.

With firmware, designers can create new features tailored for the 1980A/B. The HP 19811A Plot/Sequence ROM, used with the 1980A/B's probe, is an example. It allows the user to program a sequence remotely, specifying up to 25 keystrokes for each front-panel input. The sequence specified for a particular input may then be executed by pressing a button on the probe attached to that input. Possible future ROMs include preprogrammed test sequences with step-by-step instructions to the operator via the CRT character generator and without an external controller. Resident firmware does not refer to an option by name or number. Instead, identification is contained in the option's ROM. When the option menu is pressed, the mainframe checks for the existence of each option by checking a known memory location. If the option exists, then the option menu is written according to the ASCII string that resides in the option ROM and is displayed on the CRT.

Feature ROMs are accessed through the softkey menus. During the main program, all options and features are allowed to respond to any rotary control motion or front-panel keystrokes. As controller library routines are developed, it will become possible to transfer popular utility or measurement programs to the 1980A/B's side of the bus to minimize bus traffic and enhance overall performance. Feature ROMs will also allow expansion of the HP-IB command set.

The possiblilities for future expansion are extensive because the system directly or indirectly polls all enhancements and the enhancements may be either ROM or expansion modules that contain ROM. In addition, design changes within the system itself, such as substituting another type of interface for the HP-IB, are possible because of the partitioned architecture.

-William Watry

Table II
Sweep Range Data

Input Data Bits	Sweep Speed	Ramp Capacitor*				Current Source
0 1 2 3	time/div	100 μF	1 μF	0.01 μF	50 pF	
0 0 0 0	0.1-1 s	IN	IN	IN	IN	×1
0 0 0 1	0.01-0.1 s	IN	IN	IN	IN	×10
0 0 1 0	1-10 ms	OUT	IN	IN	IN	×1
0 0 1 1	0.1-1 ms	OUT	IN	IN	IN	×10
0 1 0 0	0.01-0.1 ms	OUT	OUT	IN	IN	×1
0 1 0 1	1-10 μs	OUT	OUT	IN	IN	×10
0 1 1 0	0.1-1 μs	OUT	OUT	OUT	IN	×1
0 1 1 1	0.01-0.1 μs	OUT	OUT	OUT	IN	×10
1 0 0 0	5-10 ns	OUT	OUT	OUT	OUT	×10

*There is always a 50-pF capacitor in the circuit in addition to the ones switched in.

controlled by the microprocessor via the main sweep DAC channel and the delayed sweep DAC channel. These DAC voltages can be varied continuously from their minimum to their maximum values. Therefore, the current sources are continuously variable and the 1980A/B's sweep speeds are continously calibrated.

Trigger Flag

To complete the control loop needed for automated measurements, the horizontal system must be able to talk back to the microprocessor. The horizontal hybrid interface provides a method of setting sweep ranges and delay time as well as a means of reading trigger conditions (trigger flag). Trigger flag is a feedback line from the sweep hybrid to the horizontal hybrid interface on the microprocessor board. This feedback line provides a flag from the trigger circuit to the microprocessor and allows the microprocessor to control the analog section interactively. This is the only time in normal operation (i.e., not during calibration) that data is transferred from the horizontal system to the microprocessor. Trigger flag is set if a trigger event occurs during the delayed sweep. The trigger source can be selected as either main trigger or delayed trigger. Using the programmable trigger source and time windows established by the delayed sweep gate, the trigger flag tells the microprocessor if a trigger event has occurred within the programmed time window.

It is the trigger flag that takes the 1980A/B out of the realm of a microprocessor-controlled oscilloscope and into the realm of a truly automated instrument that can detect signal conditions and self-adjust accordingly. The trigger flag is an integral part of the Autoscope routine, one of the 1980A/B's most significant features.[1] The 8085 microprocessor firmware controls virtually all internal states of the 1980A/B. Using trigger flag, the settings of certain modes and values may be altered by means of an algorithm that includes the parameters of an external signal. In this way, the 1980A/B may be set up to display an input signal automatically. This is the function assigned to the **AUTOSCOPE** key.

Pressing the **AUTOSCOPE** key causes the 1980A/B to examine an input waveform, adjust its settings, and present a signal approximately three divisions high and two cycles wide on the CRT. There is also a Selective Autoscope function, which is accessed through the blue prefix key, that retains previously selected setup functions such as 50Ω inputs and trigger conditioning.

Vertical System

The vertical system in a conventional oscilloscope functions as an amplitude conditioner. Because an oscilloscope must handle a large range of input signals, from millivolts to tens of volts, it is necessary to attenuate incoming signals to keep them within the dynamic range of the vertical amplifier. The vertical system must also delay the incoming signal so that the leading edge of a fast-rise pulse can be displayed on the CRT. It also provides a sync pickoff from the vertical signal which allows internal triggering, and it adds a position signal to allow convenient display of the signal.

Incorporating a microprocessor into an oscilloscope does not functionally change the vertical system block diagram. Fig. 5 shows the 1980A/B's vertical system. However, some different circuit and control implementations were incorporated to accommodate programmability. The basic building blocks of the vertical system of the 1980A/B are the attenuator, the preamplifier, the delay line driver, the delay line, and the output amplifier.

The major challenge of the vertical system was the design of the attenuator switches. They had to meet all of the electrical performance requirements of their mechanical predecessors, such as low contact resistance, low leakage currents, low input capacitance, low feedthrough capacitance, and high breakdown voltage, and they also had to be programmable. Programmability added a significant new constraint because of the electronic interface required and the increase in contact life demanded of an HP-IB-controlled instrument. The attenuator in a manual oscilloscope might see 50,000 cycles in a year of service while the attenuator in a programmable unit might see well over a million cycles within the same time period.

After a number of false starts using various types of off-the-shelf relays, and considering the natural extension of programming a cam-actuated mechanical attenuator via a step motor, a custom multiple-solenoid design seemed to be

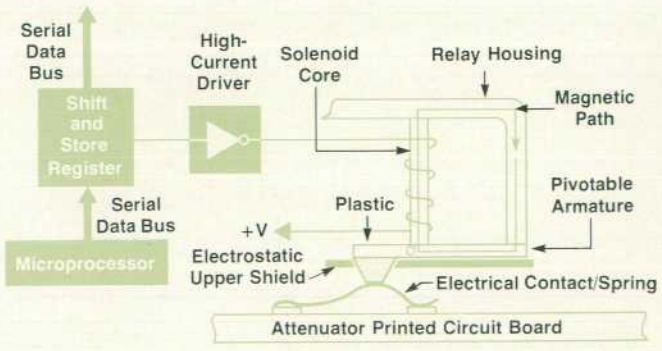

Fig. 6. *Diagram of the attenuator switch, an important element of the 1980A/B's vertical system.*

the right approach. Although this approach appeared simple, it did present a substantial set of problems.

Electrically, the attenuator has to provide a high-impedance (1 MΩ) or 50Ω termination, ac or dc coupling, ground reference, and attenuation of ×1, ×10, and ×100. This means that each attenuator needs eight contacts. Because of the space constraints of the mainframe, a dual attenuator package that includes both vertical input channels was chosen. The resulting design for a single contact is shown in Fig. 6.

The microprocessor controls the attenuator through the serial data bus. The outputs of the shift and store registers of the serial data bus interface to high-current drivers which control the individual solenoid coils. When a coil has been energized, it sets up a field in the magnetic circuit, which consists of the solenoid housing, the coil core, and the armature. The armature pivots in the electrostatic shield and forces the electrical contact/spring to make contact with the printed circuit board.

The electrical contact/spring, a critical component of this design, serves two functions. It is the signal path when activated, and the armature return spring when the coil is no longer energized. Springs on printed circuit boards are a common method of attenuator switching. However, the springs normally used are not designed for millions of cycles. Such a spring has to have extremely high tensile strength, good fatigue resistance, low tarnishing properties, high electrical conductivity, and reasonable manufacturability. To provide the amount of motion required of this spring without too much stress, the spring material needs a low modulus of elasticity as well. At first glance, berillium-copper seemed the proper material. However, this material does not have the fatigue properties needed, and it also tarnishes. An alloy of palladium, platinum, gold, and silver met all the requirements. To maintain low stress, the spring is long and thin, and to provide adequate return force to the armature, it is wide.

As mentioned earlier, the magnetic path of the relay includes the housing, core, and armature. When the coil is energized, the armature pushes the spring down by pivoting around the core. The force must be quite high to overcome the force of the spring, and so a relay material with high permeability is used. When the coil is turned off, the current ceases to flow, and the return force of the electrical contact/spring overcomes the diminishing force of the armature and breaks electrical contact with the printed circuit board. The return force also overcomes a residual magnetic force that exists after the current is switched off. This force is minimized by putting a thick chrome plating on the armature. The plating acts as an air gap in the magnetic circuit and reduces the activation force at the end of the armature's travel. Reducing this force diminishes the unwanted high acceleration that wears out the armature and decreases contact/spring life.

The reliability of the contact system was recognized as critical. During the design cycle, the contact system was severely tested. The results of these tests were used to modify the design and production processes until the desired

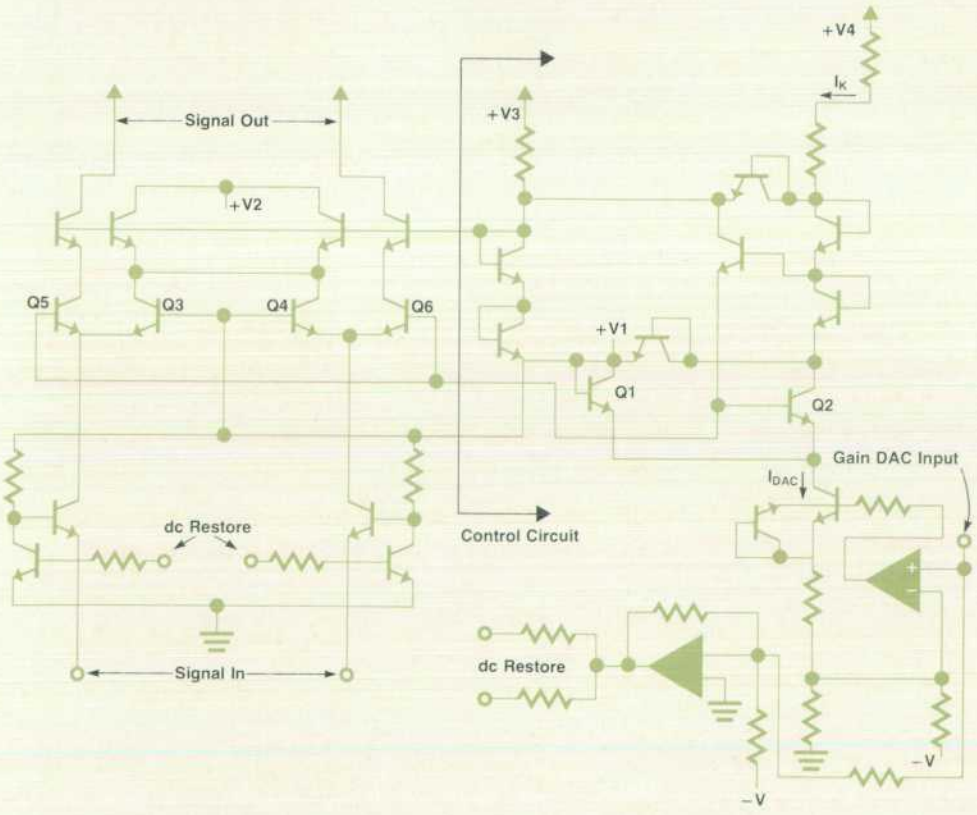

Fig. 7. *10:1 vernier design eliminates the 1,2,5 intermediate switching found in most oscilloscopes and allows continuous calibration of the vertical system.*

performance was achieved. The tests also showed that fewer than 0.6% of the contacts break in the first 1,000,000 cycles of operation. Useful life of the contacts is limited to around 1,500,000 cycles by the buildup of nonconducting organic polymers, which begins to increase contact resistance at this point.

In addition to fulfilling its function as an attenuator, the programmable attenuator designed for the 1980A/B also contributes in other areas. Primary among these is that it allows the microprocessor to scan through the vertical attenuation ranges automatically to perform automatic setup for bench applications. Second, it allows remote setup for bus-controlled applications. Third, the attenuator's input BNC connector has not only the usual signal and ground paths, but also a third path, which has two uses. One is to sense the value of a resistor in HP 10080-Series probes. If the resistor identifies the probe as a ÷10 probe, the microprocessor scales the volts/division readings on the CRT and LED displays so that the correct values are displayed. These probes also have a button that shorts the internal resistor to ground; this can be used to initiate a measurement sequence stored in the 19811A Plot/Sequence ROM (see box, page 9).

The circuit implementation of the remainder of the vertical system is identical to earlier designs except for the preamplifier and the interface level shifting necessary for electronic control. The design of the preamp is centered around a 10:1 vernier. This particular design eliminates the 1, 2, 5 intermediate range switching normally required for an oscilloscope and allows continuous calibration of the vertical system. No down-vernier, uncalibrated conditions exist for the 1980A/B.

Fig. 7 is the schematic design of the vernier circuit. Conceptually, the current I_K and the current I_{DAC}, which is generated from the gain DAC input, establish the emitter currents of devices Q1 and Q2 in the control circuit. Device Q1 in turn establishes a base voltage for devices Q3 and Q4 while device Q2 sets the base voltage for devices Q5 and Q6. By appropriately controlling the differential base-emitter voltage of these devices, the 10:1 vernier range can be achieved. The actual vernier range is approximately 12:1 to allow for calibration range. The dc restore circuit keeps the dc bias level at the output of the vernier (collectors of Q5 and Q6) constant, independent of the vernier setting.

Continuous calibration lets the user set up a convenient display that is always calibrated. For example, the vertical sensitivity may be adjusted so that the peak-to-peak display of a signal of unknown amplitude covers ten divisions. The signal's peak-to-peak amplitude is then easily determined by multiplying the displayed vertical sensitivity by ten. If the vertical sensitivity display reads 38.9 nV/div, the signal's amplitude is 389 nV.

Vertical position is also controlled by one of the microprocessor-controlled DAC channels. This particular DAC output is a current and drives the circuit shown in Fig. 8. The voltage developed at point A is reflected to point B thus controlling the total position current available from the current source. The advantage of this circuit implementation is that it uses diffused monolithic resistors and does not have to rely on precision thick-film resistors for position accuracy. Like all analog functions on the 1980A/B, the vertical position is calibrated; calibration of the vertical position is the hardware basis for the front-panel ΔV feature. When under bus control, the waveform can be positioned wherever desired, without an operator. Production test applications will find this useful.

Trigger System

An oscilloscope's trigger system selects the trigger source, internal or external, and conditions the selected signal by filtering. The trigger system provides ac or dc coupling and low-frequency or high-frequency rejection. Internal trigger source selection picks off a sync signal from one of the vertical input channels, while external source selection uses an external source input different from the vertical channels. Trigger view, which allows the user to view this conditioned trigger signal, aids in determining the trigger point. The output of the trigger system is a start-of-sweep signal for the horizontal system.

Adding programmability to an oscilloscope left the role of the trigger system unchanged. In fact, the only major

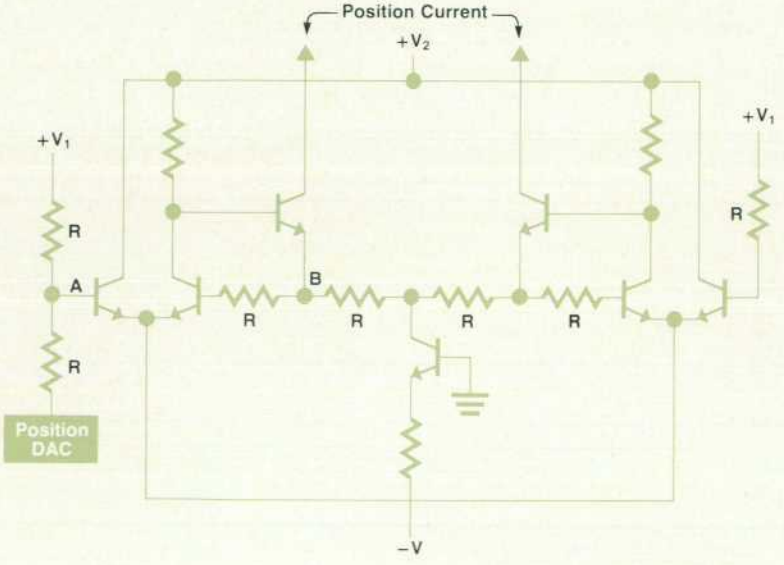

Fig. 8. *Vertical position circuit uses diffused monolithic resistors. With this circuit, a displayed waveform can be placed wherever desired without the aid of an operator when the 1980A/B is under bus control.*

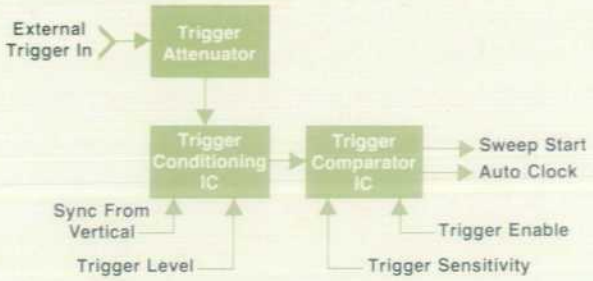

Fig. 9. *1980A/B trigger system block diagram.*

innovation in the 1980A/B's trigger system is in the interface implementation, which allows the trigger system to be controlled by the microprocessor system via the serial data bus. For external trigger inputs, the attenuator used is similar to the one used in the vertical system but with attenuation factors of ×1 and ×10 only.

The block diagram of the 1980A/B trigger system appears in Fig. 9. The three main functional blocks are the trigger attenuator for external inputs, the trigger conditioning IC for filtering the trigger signal, and the trigger comparator IC, which with the enable signal from the horizontal system generates the start-of-sweep signal.

Both the trigger conditioning IC and the trigger comparator IC are on a single thick-film hybrid circuit. Thick-film capacitors are used for implementing the filtering functions. Only the ac coupling mode requires circuitry outside the hybrid because of the size of the capacitor required.

Calibrated trigger level, one of the 1980A/B's special features, is provided by the trigger coupling IC. This feature lets the user preset the trigger level for bus-controlled applications. This is particularly valuable in production applications where the system under test has known characteristics and the trigger level can be preset without operator assistance.

The trigger comparator IC has two innovative features. The first of these is trigger sensitivity selection. Having two trigger sensitivities optimizes trigger performance as a function of vertical sensitivity. The lower trigger sensitivity corresponds to the high vertical sensitivity range (2 mV/div to 9.99 mV/div). This means that larger displayed signals are required to trigger the 1980A/B when it is on the 2.0 mV/div to 9.99 mV/div range than when it is on the 10.0 mV/div to 10.0V/div ranges. The ratio of trigger sensitivities

John R. Wilson

A native of San Luis Obispo, California, John Wilson joined Hewlett-Packard in 1978 after receiving his BSEE degree from the University of California at Davis. He has worked on the 1980A/B's attenuator and contributed to the attenuator section of this article. His interests include kayaking, tennis, soccer, downhill and cross-country skiing, and photography.

William E. Watry

Bill Watry, software project leader in the oscilloscope R&D lab, has written a significant portion of the 1980A/B firmware including system expansion capabilities and the routines that interface the keyboard and rotary control. Bill recently assumed the management supervision of a laboratory group that is developing 1980A/B applications software. He has a BSEE degree, specializing in computer science, from the University of Colorado in Colorado Springs. Bill joined HP in 1966 and has worked on oscilloscopes for 16 years. He is married and has five children. He coaches and plays soccer and enjoys motorcycling and skiing.

Russell J. Harding

Russ Harding joined HP in 1968 after receiving his BSEE and MSEE degrees from Purdue University. He has worked in the sampling oscilloscope group, the displays group, and the monolithic IC lab. After joining the 1980A/B project team, he was responsible for the design of the attenuators and trigger circuits. He then became project manager for the hardware design, and later transferred with the 1980A/B to production as production section manager. Russ is married and has a daughter and a son. In his spare time he hikes, cross-country skis, collects beer advertising memorabilia, and works on his son's model train.

Wilhelm Taylor

After receiving his BSME degree from Colorado State University, Will Taylor joined HP's Colorado Springs Division in 1975. He has worked on the 1980A/B project and the 1950A expansion module for the 1980A/B. Will is currently with HP's Colorado Telecommunications Division and has an MBA from the University of Colorado in Colorado Springs. His hobbies include running, chess, and woodworking.

Monte R. Campbell

Monte Campbell, presently project manager for the 1980 A/B's expansion modules, worked on the horizontal system integrated circuits in the 1980A/B. Monte, who joined HP in 1977, has a BSEE degree from Colorado State University and an MSEE degree from Stanford University. He is married, has a daughter, and lives in Woodland Park, Colorado. He has a private pilot's license and enjoys softball and skiing.

is 2 to 1. This difference helps reduce the possibility of triggering on noise when using the high-sensitivity vertical ranges.

The other feature of the trigger comparator IC is the auto clock output. This output is a shaped version of the input signal that is sent to the horizontal system. There it is combined with other signals to generate the trigger flag signal essential to the 1980A/B's Autoscope operation and other trigger flag measurements.

Reference

1. P. Austgen, W. Watry, and M. Karin, "Software-based design automates scope operations," Electronics, March 10, 1981, pp. 181-188.

The Early History of the 1980A/B Oscilloscope Measurement System

by Zvonko Fazarinc
Hewlett-Packard Laboratories

The development of the 1980A/B Oscilloscope Measurement System began many years ago when John Young, then an HP vice president, approached Paul Stoft, director of the Electronic Research Laboratory, with a request for a concerted effort in the field of oscilloscopes. The explorations were to pursue the trends in time-domain measurements in view of the emerging digital electronics.

During the ensuing weeks a series of brainstorming sessions were conducted by Paul Stoft and attended by members of the technical staff. The Colorado Springs Division, which is responsible for oscilloscope development and manufacturing at Hewlett-Packard, sent representatives to Palo Alto, among them the present division manager, John Riggen.

The enthusiasm for what we called the "smart scope" grew quickly in the laboratory and exciting new ideas were generated at a high rate in a synergistic exchange between the traditional analog engineers and the digitally oriented team that had just completed the development of the first scientific pocket calculator, the HP-35. Eventually Paul Stoft felt that the time was ripe for organizing the project team and charged this author with the task.

First, the critical areas were staffed. Dan Hunsinger, presently the IC facility manager of HP's Santa Clara Division, was given responsibility for inventing and developing the voltage-controlled preamplifier. His effort resulted in proprietary designs that dealt successfully with noise and control linearity problems over two decades of gain. Dick Baumgartner, who had experience with oscilloscope design, was given the task of solving the voltage control problem for the sweep generator. Dick Crawford, the most experienced of all, who had been coordinating the whole effort within the laboratory and with the division up to that point, was charged with responsibility for deflection amplifiers, power supplies, and packaging. Because we wanted to keep the beam intensity under processor control, he was also faced with the problem of the DAC interface to the high-voltage supply. Dave Cochran, who had just developed and implemented the scientific library for the HP-35 Calculator, accepted responsibility for the control algorithms and for the display driver circuitry.

Wayne Grove joined the team as the liaison to divisions that would be involved in integrated circuits, hybrids, LED displays, and other components. Greg Justice was to develop a low-power vertical deflection amplifier and Jim Umphrey and Bill Mordan, whose talents were contributed by the Colorado Springs Division, were to develop the digital delay and the trigger circuit, respectively. Mark Morgenthaler joined the project to work on the attenuator but was soon charged with the development of a voltage-controlled delay generator and of a precise triggerable oscillator. Ken Peterson took on the responsibility for the delay counter. The number of controlled blocks grew quickly beyond the practicality of individual digital-to-analog converters, so Knud Knudsen was given the responsibility for a 16-channel single-chip DAC. Rich Wheeler's task was to adapt a magnetic card reader for storage of control settings. When Ralph Eschenbach accepted the task of system partitioning into hybrids and the development of the required substrates, the project seemed to be well on its way with the exception of the digital controller. This problem was resolved when Francé Rodé, the developer of the HP-35 processor, responded to the challenge of making his processor do the controlling function and joined the team.

The tremendous strength and dedication of the project team resulted in fast progress in circuit development but also in an even faster proliferation of ideas that mercilessly ignored the traditions in oscilloscopy. Serious questions of market acceptance arose and we decided to subject the new concepts to the scrutiny of management, marketing, and representative users in the form of a computer simulation. Paul Hughet, coached by Jim Duley, produced a complete emulation of controls and responses on an HP computer. This was used successfully to test a number of competing ideas and provided a good preview of the proposed concepts for management. A project review by top corporate and divisional management, which included a functional mockup of the oscilloscope tied to the computer by an umbilical cord, brought full support for the project and a number of good suggestions, most of them from Barney Oliver, HP vice president for R&D, who was actively involved in the project throughout its life. A number of excellent suggestions came from division management, notably that for a single control knob with menu selection and character generation on screen as an alternative to individual pushbutton controls and LED displays.

Responsibility for the breadboard rested with Frank Lee, Rich Marconi, Lyman Miller and Gene Reynolds. They not only kept pace with numerous changes but continually upgraded the functional breadboard with custom integrated circuits as these were processed by the Santa Clara bipolar facility and by Loveland's MOS processing plant. During this period the industrial designers, Bill Wohltman and Dick Anderson, produced a line of attractive packages for the instrument, and George Drennan, Bob Hirsch, and Dan Paxton worried about the mechanical aspects of internal packaging in preparation for tooling design. Clarence Studley, the designer of the HP-35 keyboard, took another look at the same problem from the instrumentation viewpoint and generated a number of innovative ideas. The lion's share of the effort, though, was devoted to software. The newly acquired dimension of freedom unleashed the imagination of the project team and of oscilloscope users. Proposals for digital calibration, automatic balance adjustment and automatic setup of controls originated from Francé Rodé, Ralph Eschenbach, Pete Lindes, and Tom Hornak.

The need for closer coordination in view of the approaching transfer of the project induced the Colorado Springs Division to name Stan Lang as the responsible project manager. In the ensuing year the ties between the laboratory and the division strengthened through the goodwill of Stan and his team. After a visit by Bill Risley it became clear that the lab's role in the project was quickly nearing its end. A few months later the project was transferred.

The Design and Development of the 1980A/B at Colorado Springs

by William B. Risley
Colorado Springs Division

After the 1980A/B Oscilloscope Measurement System was transferred to Colorado Springs, a substantial team was assembled to complete the design efforts. Walt Fischer, who is now marketing manager of HP's Colorado Telecommunications Division, was the R&D section manager with Tom Bohley, Stan Lang, and the author as project managers. Tom was responsible for the overall circuit design and packaging, and Stan handled the system design. My group was responsible for the processor system and firmware. The programmable attenuator was contributed by Russ Harding, Wilhelm Taylor, and John Wilson. Eldon Cornish contributed the preamplifier and vertical output stage, and Marvin Estes helped support the vertical system design and developed probes. Roy Wheeler completed the digital-to-analog converter circuits and hybrid and designed the gate and high-voltage power supply. Russ Harding, Jim Umphrey, Eldon Cornish, Monte Campbell, and Dennis Weller all contributed to the trigger and time base. Paul Austgen, Dick Tabbutt, Bob Landgraf, Bill Watry, Mike Karin, and Fred Rampey developed the processor system and firmware.

The package, front panels, and numerous parts were designed by John Campbell, Carolyn Finch, Jim Carner, Ernie Hastings, and Wilhelm Taylor. Tom Bohley and Jim Felps developed the power supply, and Don Skarke and Joe Millard worked out the thermal management for the product. Near the end of the project, Ed Evel, Ken Rush, and Al Best helped resolve system problems resulting from putting a noisy processor into a highly sensitive instrument.

Ray Kushnir, Don Smith, Roy Wheeler, Tom Bohley, Ron Westlund, Chuck Small, and Larry Gammill all provided significant refinements and guidance in the transfer of the 1980A/B to production. Bill Ford, Johnnie Hancock, and Rod Schlater also contributed their skills to the transfer of the product to manufacturing. Jim Williams was the industrial designer and was assisted by Don Henry and Mike Easter.

There were many others without whom the project could not have been completed. Among these were the persistent engineers in the IC facilities at the Colorado Springs, Loveland, and Santa Clara Divisions, those in printed circuit design and fabrication in Colorado Springs and Loveland, and the process and production engineers who had to learn how to build the novel front panels and attenuators.

Digital Waveform Storage for the Oscilloscope Measurement System

by Eddie A. Evel and Robert M. Landgraf

WITH THE ADDITION of digital waveform storage, the 1980A/B Oscilloscope Measurement System, which on its own is fully programmable, can be operated completely through a controller without human interaction. With the basic 1980A/B, data can be acquired using the continuously variable trigger level, trigger flag, and HP-IB controller software. However, this data cannot be displayed on the CRT screen. With the 19860A Digital Waveform Storage Option, digitized data can be displayed on the CRT and sent to a computer for analysis, and waveform data created by the computer can be displayed on the CRT. Although the 1980A/B's trigger flag used with external software can digitize waveforms, additional software is not needed with the 19860A.

The 19860A Digital Waveform Storage Option increases the overall usefulness of the 1980A/B by digitizing one or two displayed waveforms and storing them within the instrument for later display or for data output on the HP-IB. With this feature the 1980A/B can contribute to fully automatic applications. The HP-IB system controller can automatically analyze the digitized waveform data and perform go/no-go tests on complex signal waveforms, automatically adjust the device being tested, or instruct the operator. The 19860A lets the bench user store waveforms for future reference and obtain data output for bench applications. In addition to outputting data to a calculator or computer, the 19860A can output data directly to a plotter to obtain hard copy without the aid of a controller. Low-repetition-rate data or in some cases single-shot data that normally cannot be observed on a conventional oscilloscope can be digitized and displayed.

Fig. 1. *1980A/B option menu panel with 19860A Waveform Storage option installed.*

1980A/B-19860A Interaction

The 19860A hardware is designed to use and enhance the capabilities and features of the basic instrument. For example, since the 19860A digitizes waveforms on the 1980A/B's CRT screen, it uses all signal conditioning done by the 1980A/B, such as amplification, bandwidth limit, positioning, and channel switching. Also, the 19860A uses the delay sweep timing circuitry within the 1980A/B sweep circuitry as the time base for the digitizing operation. The 1980A/B's microprocessor controls the digitizing operation and does the data scaling and data input/output.

The digitizer option consists of a sample-and-hold cir-

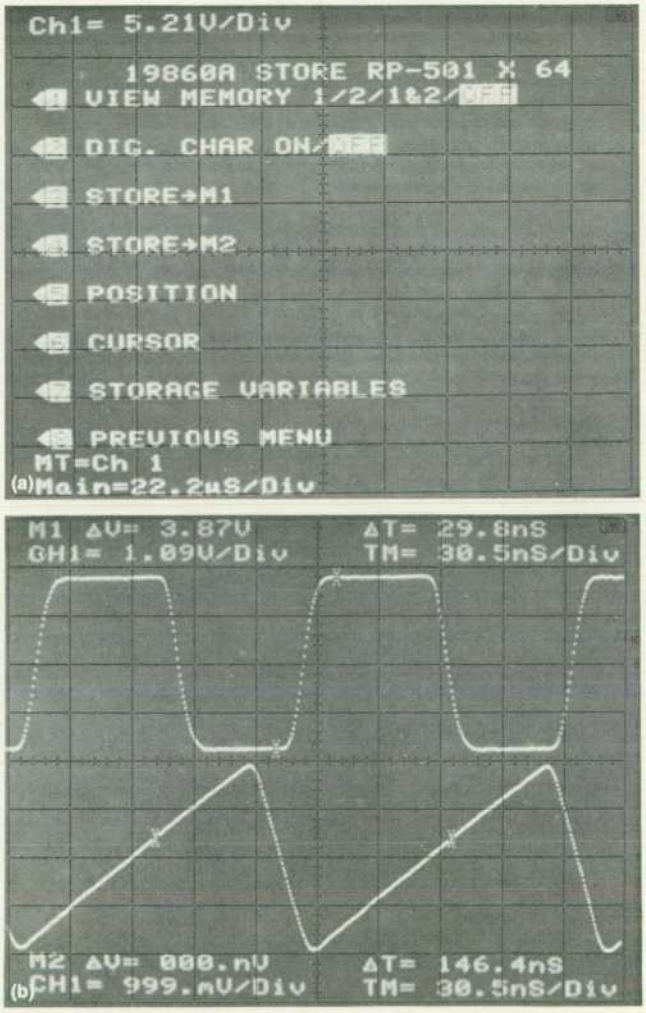

Fig. 2. *(a) Waveform storage menu. (b) Cursors positioned on digitized waveforms with time and voltage differences displayed.*

cuit, an analog-to-digital converter (ADC), data storage and display memory, two display digital-to-analog converters (DACs), and control logic. Fig. 3 illustrates how the 19860A digitizer is integrated into the 1980A/B system.

The 19860A expands the 1980A/B through two plug-in cards internal to the mainframe. One of the cards contains 2K of ROM and 1K×12 bits of data display RAM. An additional 8K of ROM uses two feature-ROM slots in the mainframe, and 384 more bytes of 1980A/B system RAM is available to the two occupied feature-ROM slots.

The 8085 system microprocessor executes restart commands that link the expansion blocks to the mainframe functions, which are shared. The restart command followed by a table number allows an effective subroutine jump to a specific, table-defined subroutine. The restart command links the mainframe to the expansion module, feature ROMs, and internal expansion cards and allows interlocking the rotary control. Cleanup routines resulting from key execution also connect with the expansion blocks. The information required to keep track of whether the signal source requires repetitive or real-time sampling is handled through the restart system as the instrument settings are changed. The expansion cards and expansion module each have different restart codes. Before the subroutine is read, an existence check is made to determine if the particular expansion block is contained in the instrument. If not, an immediate return is executed. (Also see page 21 for a discussion of mainframe/option interaction.)

As shown in Fig. 3, an incoming signal goes through the vertical preamplifier, the delay line, and the vertical output amplifier to the CRT. At the same time, the signal is sent to the trigger circuit. A trigger is generated and used by the horizontal sweep circuit to initiate a sweep ramp. This goes through the horizontal output amplifier to sweep the beam across the CRT, thus generating the real-time trace.

As the first step in the digitizing operation, the instrument checks for a valid, digitizable signal and for a valid operating mode. Invalid modes include the dual horizontal mode, which displays both main and delayed sweeps, and the digital delay and trigger delay modes. Advisory messages indicating invalid modes are displayed, thus eliminating the need to refer to an operating manual for the meaning of error codes.

At the start of the digitizing routine, the microprocessor shuts down the interrupt system and terminates the character display so that only the signal source to be digitized is displayed during the storage operation.

During a digitize operation, the signal out of the vertical output amplifier is also fed to the sample-and-hold circuit. At the appropriate time, the sample timing signal is issued by the horizontal sweep circuit. This causes the sample-and-hold circuit to take a sample. Then an A-to-D conversion is done and the data is loaded into the data storage and display memory. Once the microprocessor senses that the data point has been loaded into memory, it programs the horizontal sweep for a new sample time. Then the sample-and-load-memory cycle is repeated until as many as 501 data points on the waveform are stored into memory. Later, the data may be displayed back on the CRT using the X and Y display DACs. The DAC outputs are multiplexed onto the CRT during the character generator display cycle.

Data is sampled at the output of the CRT driver to allow a

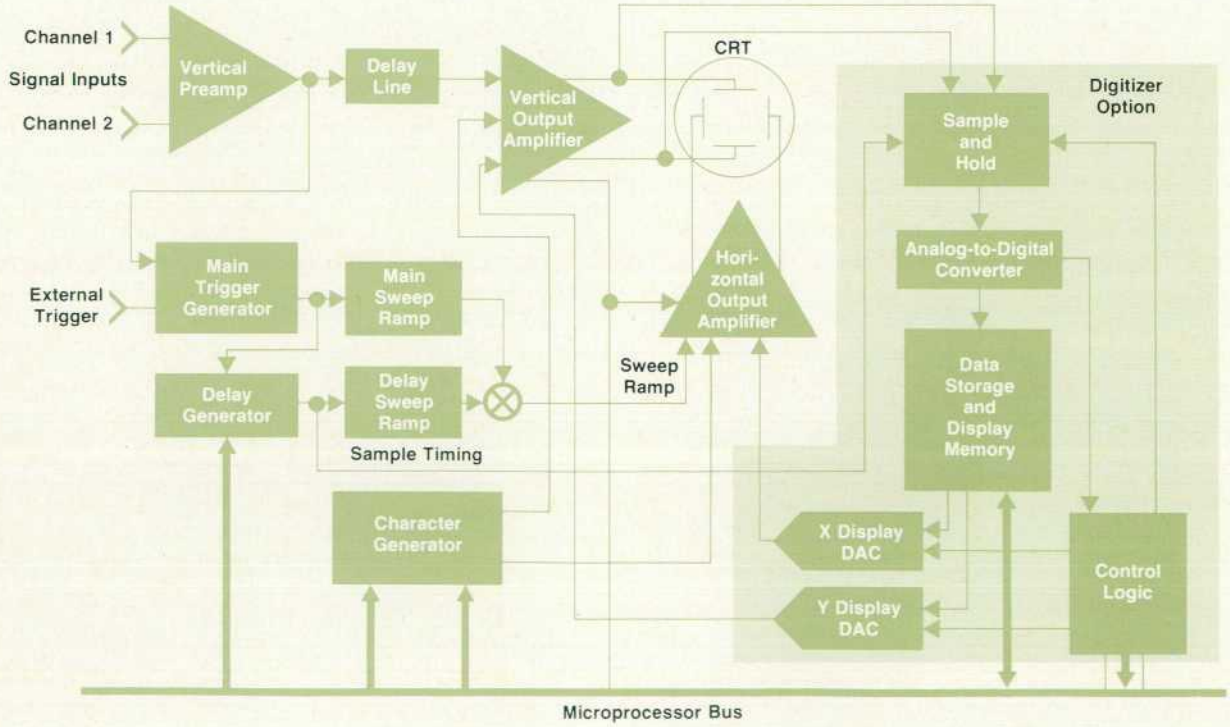

Fig. 3. *Block diagram of the 19860A Waveform Storage Option for the 1980A/B Oscilloscope Measurement System. The option digitizes one or two displayed waveforms and stores the data for later display or output on the HP-IB (IEEE-488).*

frequency response equivalent to the CRT display. Individually acquired digitized signals are stored in one of two local data memories. Each memory contains 501×12 bits, each 12-bit data word consisting of 10 bits of data, one bit for display blanking control, and one bit that is not used.

Status of the digital storage operation is reported over the HP-IB. The report includes completion of a digitizing operation, information equivalent to the CRT-displayed advisories, and information regarding the possible clipping of a signal positioned partially off screen. Thus, the information seen on the CRT is available to a computer for complete automation.

Repetitive and Single-Sweep Sampling

At the faster sweep speeds, the 19860A uses a repetitive sampling technique in which the signal to be digitized is sampled at different times during successive occurrences of the signal. Two sweeps per stored data point are used. The specific sampling times are determined by the sweep speed setting of the 1980A/B and the number of points selected to be digitized. The signal is sampled at each point by the narrow aperture of the sample-and-hold circuit, then an analog-to-digital conversion is made, and data is loaded into the memory. This method enables the 19860A to obtain ten-bit data on very fast signals (up to 100 MHz) while using a low-cost, low-power-consumption ADC. It also allows time resolution down to 100 ps between data points.

At sweep speeds slower than 1 ms/div, the minimum time between data points is greater than 20 μs (determined by the maximum 501 points for ten divisions of horizontal display). This allows the 19860A to switch over automatically to a single-shot mode. In this mode, the 19860A starts sampling the signal when the 1980A/B is triggered, and up to 501 data points are taken on one occurrence of the signal. This mode operates like the repetitive mode, except that a programmable counter is started when the sample timing signal occurs (Fig. 4). The microprocessor programs the counter to count down starting from the value of the next time increment between data points. Each time the counter reaches zero, a sample is taken. The result is that the timing signal takes the first sample and starts the counter, which takes all successive samples on one occurrence of the waveform.

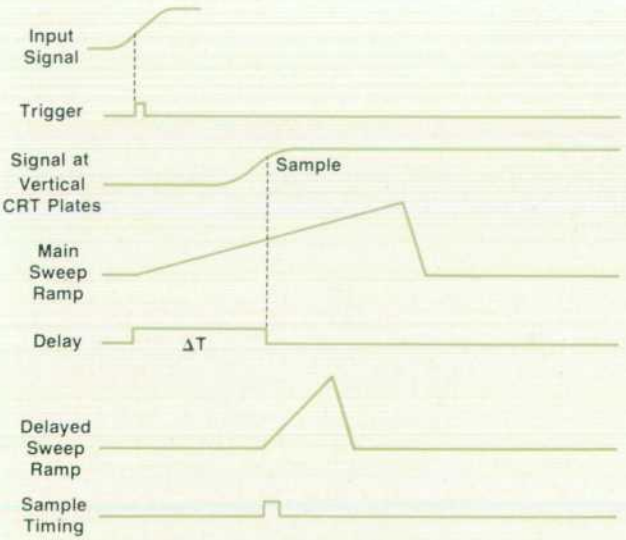

Fig. 4. *Timing for sampling a waveform to be digitized is generated using the 1980A/B's sweep delay.*

Compared to a "flash" ADC, this method is much simpler, uses less power, and is a proven design. It requires less hardware and is cheaper to implement. For repetitive signals, it offers much higher bandwidth and much better timing resolution than a flash converter.

Sample Timing

The basis of the sample timing system is the microprocessor-controlled sweep timing circuit. The sample timing signal is generated through the oscilloscope's delayed sweep mode. An oscilloscope normally uses the delayed sweep mode to generate a sweep that begins some variable time after the main sweep is triggered and started. The user selects the delay time to observe part of a waveform on a faster delayed sweep speed. Fig. 4 shows the sequence of events.

First, the trigger circuit operates on the input signal to generate a trigger based on a transition of the input signal, such as a positive-going step. The trigger causes the main sweep ramp to start sweeping across the CRT to display the waveform. A delay is also initiated. At the end of the delay, the delayed sweep ramp is started. Either the main sweep ramp or the delayed sweep ramp is gated to the horizontal output amplifier to generate the horizontal sweep at the CRT. The delayed sweep causes the CRT beam to sweep across the CRT at a different rate from the main sweep, thus producing an expanded display of a portion of the input signal.

In addition to starting the delayed sweep at the end of the selected delay, the sample timing signal is generated. If the sampler is enabled, a sample is taken. To take samples at different points on the waveform, the microprocessor need only program different delay times. The microprocessor calculates the desired time between sample points and increments the delay generator time by that amount as each sample is taken on the waveform. When the desired samples have been taken and loaded into the memory, the microprocessor returns the delay setting to its original value.

The delay generator uses a combination of analog and digital circuits to obtain a very accurate delay time. For delay increments between 0 and 100 ns, an analog delay circuit is used. For delay increments greater than 100 ns, a counter and a crystal oscillator are used to achieve high accuracy. Using this system to generate the sample timing signal increases the timing accuracy of the digitized data over that of the real-time CRT display, which is generated by an analog sweep ramp circuit.

Defining the Digitized Window

In the vertical axis, any part of the trace that is within the CRT graticule will be digitized. In the horizontal axis, ten divisions are digitized except when the 1980A/B is in the intensified sweep mode. In this case, data is taken on the part of the waveform where the intensified marker appears, but the data taken is always redisplayed over ten horizontal divisions on the CRT.

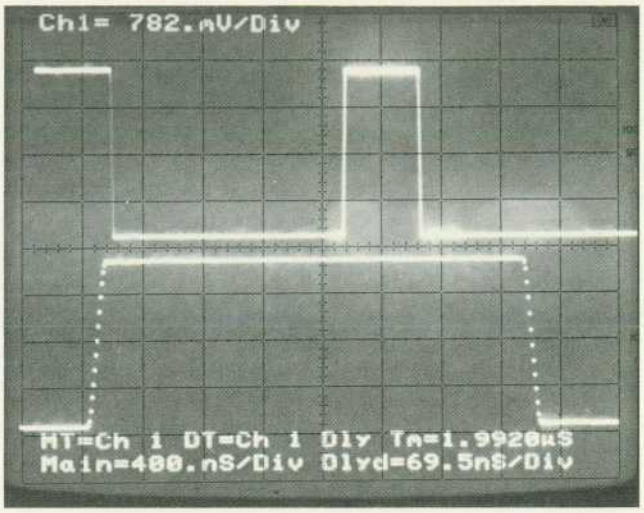

Fig. 5. *In intensified sweep mode, the digitizer samples the waveform during the intensified window, then displays this data over ten horizontal divisions.*

The sweep mode that is in effect when the digitize command is given determines the time window to be digitized. There are three possible modes: main, delayed, and intensified. In main sweep mode, the microprocessor uses the main sweep time per division to calculate the time increment needed to obtain the desired number of points across ten divisions of main sweep. The delay is set to zero for the first point and then incremented for each successive point until all points are taken.

In the intensified sweep mode, the sweep is done by the main sweep ramp, but the delayed sweep ramp intensifies the trace. This defines the region that will be viewed when the oscilloscope is switched to delayed sweep. The intensified marker also defines the portion of the waveform to be digitized. The marker length is determined by the delayed sweep time per division and is used when calculating the digitizer time increment. After taking the desired number of points during the intensified window, the digitizer then displays this data over ten horizontal divisions as shown in Fig. 5. The first digitized point is taken at an initial delay determined by the oscilloscope settings, and then the delay is incremented for successive points. In delayed sweep mode, the real-time trace is expanded on the screen around the portion of the waveform defined in the intensified mode. The delayed digitizing operation is identical to the intensified digitizing operation.

Display Cycle

Once data from a waveform is stored in the memory, it may be displayed on the CRT with or without the real-time waveform display. To do this, the microprocessor initiates a digitizer display cycle each time the character display is refreshed, approximately every 15 ms. The digitized trace, the characters, and the real-time trace are all displayed by time-multiplexing the CRT beam. The characters are displayed by using a raster scan of the CRT and modulating the beam on and off. The digitized data is displayed during the vertical reset cycle of the raster scan. During the raster scan when characters are not displayed, the real-time trace is multiplexed onto the CRT and displayed (Fig. 6). Real-time trace timing normally is asynchronous with the character display cycle; therefore, the missing segments of the real-time trace usually are not noticeable.

Character generator data display is under direct-memory-access (DMA) control. At the beginning of the last line of text display, DMA is completed. Through microprocessor interrupt, a request is made to reprogram the DMA channel. Before DMA reprogramming, the character generator interrupt service routine checks for the existence of the digitizer and a digitized data display request. Digitized data display occurs under DMA control with either one or two sections of the digitizer memory read for display. Immediately preceding data display, the intensity value of the digitized data display is sent to the intensity DAC, which is shared by the character generator and the digitizer display. After display, all modified values are restored, and reprogramming the DMA channel for character generator control continues.

How the Sample-and-Hold Circuit Works

The 1980A/B's sample-and-hold circuit, common to HP sampling oscilloscopes such as the 1810A, has a 300-MHz bandwidth, which prevents the digitizer from degrading the 100-MHz bandwidth of the 1980A/B system.

The circuit consists of a four-diode sampling gate, a holding capacitor, and a special circuit called a stretcher circuit (Fig. 7). The input signal is sampled by switching the four-diode sampling gate on for 1 ns, as shown in waveform 1 of Fig. 7. The holding capacitor is charged to about 10% of the voltage appearing at the input of the sampling gate; this is the initial transient of waveform 2. The voltage transient appearing across the holding capacitor is amplified and

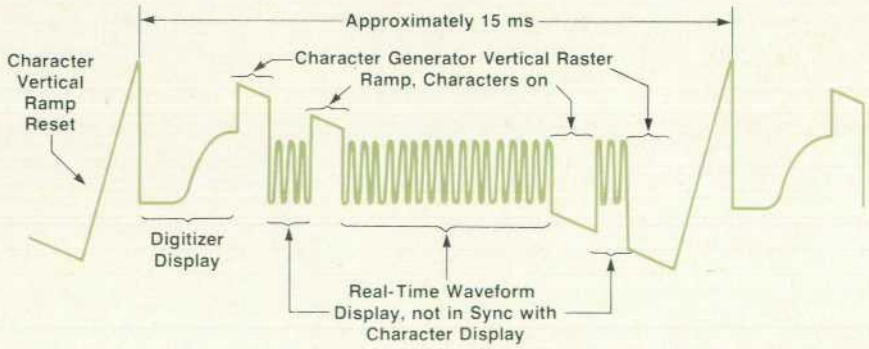

Fig. 6. *The signal applied to the CRT's vertical deflection plates has the digitized trace multiplexed with the characters and the real-time trace.*

stretched by pulse-shaping circuitry in the stretcher amplifier. The resulting transient voltage, waveform 3, is gated to an operational-amplifier integrator circuit by turning on the FET with a pulse, as shown in waveform 4. The resulting waveform out of the integrator is shown by waveform 5. This voltage is fed back to the holding capacitor, which is charged to a new level which is the same as the momentary input voltage when the sample was taken. The voltage is held at a constant level by the integrator until the next sample is taken.

For the second sample, if the applied input voltage is the same as when the first sample was taken, there is no voltage transient on the holding capacitor and no change in the output of the integrator. However, if the integrator voltage resulting from the first sample was slightly erroneous, a transient across the holding capacitor results. This transient is proportional to the difference between the true input voltage and the incorrect voltage resulting from the first sample. The transient is processed through the stretcher circuit so that the integrator output charges towards the correct value. Any error between the input voltage and the integrator output voltage is quickly nulled out after a few samples.

If the input waveform is changing, any error is proportional only to the voltage difference between one sample and the next. Typically, the error is less than 1% of the voltage change between sample points, resulting in extremely accurate data as long as enough samples are taken on a transient input waveform.

Since the four-diode gate is switched on for only 1 ns, the resulting aperture time is 1 ns, giving a bandwidth well above 300 MHz.

Autocalibration

To improve stability and accuracy and eliminate the need for periodic calibration of the sample-and-hold circuit and the ADC, the microprocessor automatically calibrates the sample-and-hold and ADC circuits each time data is taken on a waveform. The calibration consists of using the display DACs, which are relatively stable, to position the CRT beam at various locations on the CRT in the vertical axis. Data samples are taken by the sample-and-hold circuit and the ADC and compared to the expected value. This information is used to generate gain and offset correction factors that are stored and later used to correct data taken on the real-time waveform. Autocalibration normally is done each time the digitize operation is initiated, before actual data is taken on the waveform. To improve accuracy, different correction factors are obtained for different segments of the screen. This calibrates out minor system distortions.

Since calibration uses most of the hardware and firmware, it doubles as a confidence test. If any hardware is not operational or manual calibration is severely out of bounds, the 19860A's automatic calibration routines can detect the problem and display advisories.

An efficiency DAC controls the gain of the fast sample-and-hold circuit used with the sampling bridge. The sample-and-hold circuit is calibrated so that it converges to a final value in one sample interval for a given signal. To calibrate the sampling efficiency automatically, a known transition must be established and digitized. The digitizer display DAC provides this transition because it is extremely stable and is manually calibrated to the CRT screen during initial setup.

The firmware uses a successive approximation routine (binary convergence) divided into two operation modes for

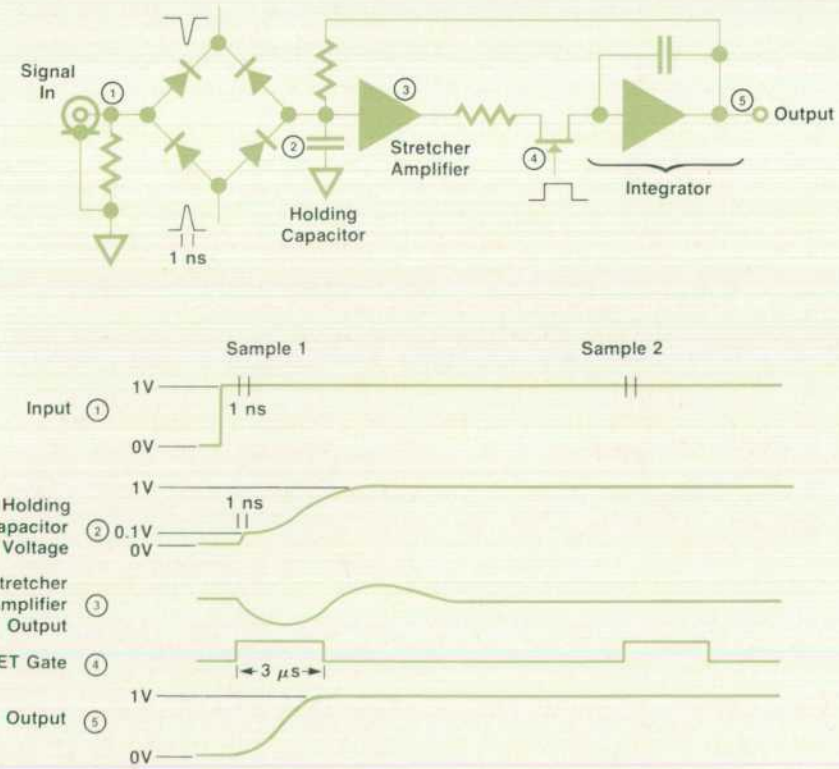

Fig. 7. *Sample-and-hold circuit and waveforms.*

optimum speed and accuracy during calibration. In the first mode, data averaging is performed only to determine the proper value of convergence; in the second mode, averaging is used to reduce the effects of noise. For a data transition of eight divisions, a point is displayed at −4 divisions and is sampled six times. This ensures that even with low gain and low DAC values, the −4 starting point will pull the amplifier out of saturation and will give a value representative of a point on-screen. Next, a point is displayed at +4 divisions. After it is sampled once, it is sampled twenty times more with the last sixteen sample values averaged to get a convergence or reference value. The initial value is compared to the averaged value, and the efficiency DAC is adjusted for the next iteration. When the difference approaches the digitizer noise level, the averaging mode is selected. The eight-division transition between −4 and +4 and the first sample acquisition at +4 are repeated 16 times. The 16 values are averaged to reduce the effects of noise before comparison to the reference value. Failure to converge to a DAC value between 1 and 255 results in an error. The DAC is set by outputting eight bits to an I/O port in a combination 2K ROM and I/O chip. As an additional confidence test, the I/O port is read to verify that the I/O chip is operating.

In the second part of automatic calibration, the correcting factors to be used during the display of digitized data are determined. A data value is corrected for display at the location where the original signal point was sampled. To accomplish this display correction, the CRT screen is divided into three sections. This is necessary because, while the center four divisions (between locations 256 and 768) are very linear, amplifier compression causes some distortion in the upper and lower two divisions. Display locations are sampled at display DAC locations 128, 256, 768, and 896 with 64 samples averaged for each location. Data is then forced to fit an equation of the form $y=ax+b$. To correct displayed data, a table of correction factors is generated that specifies correction factors for all 1024 possible values of the 10-bit DAC output. This correction table exists primarily in the character generator RAM and partially in the instrument feature RAM space. Because the character generator shuts down during the digitizing process, the buffer RAM is used as a scratchpad RAM. Checks are made to determine if the maximum correction of any point on screen is out of bounds and if the portion of the CRT screen between +4.5 and −4.5 divisions can be digitized.

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Bob Landgraf, a native of Freeport, Illinois, came to Hewlett-Packard in February of 1970 after receiving a BSEE degree from the University of Illinois. Bob worked as a hardware development engineer on the 1720A Oscilloscope project and later as a software development engineer on the 1980A/B System before joining the 19860A Waveform Storage group. Bob is single and lives in Woodland Park, Colorado. He spends his leisure time backpacking and cross-country skiing. He also enjoys amateur photography and competes locally in the Pikes Peak Camera Club.

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Ed Evel is a native of Utica, Kansas and received his BSEE degree from Kansas State University in 1962. He spent three years working on missile guidance systems before joining Hewlett-Packard in 1965. Since then he has worked on a variety of projects including oscilloscopes, probes, computer systems, an LSI logic family, and a laser trimmer for thick-film hybrids. He designed the circuits for the 19860A digitizer option and the test system for the 1980A/B thick-film hybrids. He holds three patents on electronic circuits. Ed is single and is raising two daughters from a previous marriage. He lives in Colorado Springs and enjoys photography, camping, skiing, snowmobiling, and motorcycle riding.

Putting the Measurement System on the Bus

by Michael J. Karin

SINCE THE ADVENT OF HP-IB-controlled instruments in the early 1970s, many industries have used them to assemble automatic and semiautomatic test systems.* Sources, voltmeters, and counters were the first instruments "put on the bus," and spectrum analyzers, network analyzers, power supplies, logic analyzers, and display devices soon followed. Until the 1980A/B Oscilloscope Measurement System was introduced, however, all automatic test systems lacked bus-controlled oscilloscopes. Integrating a microprocessor and an HP-IB interface into the control section of the 1980A/B transformed a conventional benchtop instrument into a measurement system.

By programming the 1980A/B from an external controller via the HP-IB, a test system designer can establish front-panel settings, communicate test procedures through the CRT display, and get measurement results from the 1980A/B back to the controller. Test procedures can be displayed step by step for the operator, thereby simplifying complex tests.

The 1980A/B has an 8085 microprocessor to control the analog signal path. This is a radical departure from the knobs and pushbuttons of other oscilloscopes. Functions and features of the front panel are not limited by the circuitry behind them but only by the ingenuity of the software designer. The microprocessor receives information from the front panel as well as from other sources, such as the HP-IB interface.

*HP-IB is the HP Interface Bus, Hewlett-Packard's implementation of IEEE Standard 488 (1978).

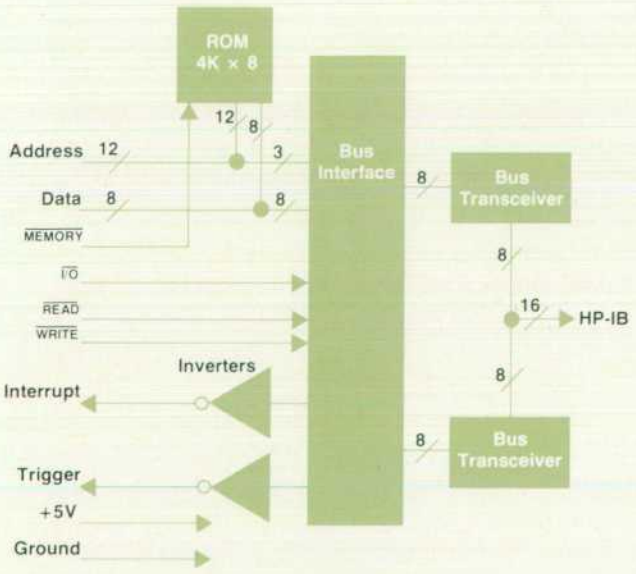

Fig. 1. *Block diagram of the HP-IB interface.*

Hardware Implementation and Electrical Interface

The 1980A/B's HP-IB printed circuit board has only five integrated circuits. There is a 4K×8 NMOS ROM, a bus interface IC, two interface transceiver ICs, and an inverter IC.

The ROM contains all the parsing, talking, interrupt service, and utility routines unique to the HP-IB. The bus interface IC implements all of the IEEE 488 interface functions except the controller function. The bidirectional bus transceivers provide the electrical interface between the interface IC and the HP-IB connector on the rear panel of the 1980A/B. The hex open-collector inverter buffers several signals from the bus interface IC to the rest of the 1980A/B. Fig. 1 is a block diagram of the HP-IB interface.

The electrical interface to the processor consists of 12 bits of address, eight bits of data, chip selects for memory and I/O, read and write control lines, an interrupt line to the processor, a trigger line that goes to the expansion module and the waveform storage, +5 volts and ground. There is also a reset line from the processor board that is active during power-up. This line is not used by the HP-IB but is available for future interfaces.

Address selection is done via a menu on the CRT display. This same menu allows selection of listen-only and talk-only operation as well as the standard addressed mode.

Fitting the Interface into the Firmware System

Although the HP-IB interface is standard in the 1980A/B, it relates to rest of the instrument like an option. This places some constraints on the HP-IB code, because options must be "removable."

Because it is designed as an option, making the HP-IB interface work with the firmware system is similar to making a plug-in expansion module or digital waveform storage work with the firmware system. There are times during an operation sequence when the option needs to take control. Putting a simple CALL instruction to the option in the code is insufficient because the option may not be installed.

The problem of determining whether the option is present and calling it was solved by using the 8085's RST instruction. The restart instruction is a one-byte instruction similar to a CALL (subroutine call) instruction, except that it branches to one of only eight locations in memory. Three restarts were defined for the three 1980A/B hardware options: RST 1 for the expansion module, RST 2 for the HP-IB, and RST 3 for waveform storage. A numeric parameter follows each restart instruction. This parameter is used as a pointer into a dispatch table near the beginning of each option's firmware. The destination of the restart instruction

Bit	8	7	6	5	4	3	2	1
Mask Weight	128	64	32	16	8	4	2	1
Service Request Condition	SRQ Key	RQS Bit	Plug-in Option Request	Internal Option Request	Advisory or Error	End of Sweep	Key Closure	HP-IB Syntax Error

Notes: 1. To set the RQS bit and SRQ bus control line true, the condition must be enabled in the RQS mask.
2. If no condition is enabled, the I980A/B cannot set the SRQ bus control line or the RQS bit true. However, bits 1-6 and 8 of the status byte are set to indicate which conditions have occurred.

Fig. 2. *HP-IB status byte and service request mask. Seven 1980A/B conditions generate HP-IB service requests; they are individually maskable.*

passes another parameter to a routine called the restart handler. This second parameter specifies the hardware option desired.

The restart handler checks to see whether the desired option is present. If it is not, the restart handler returns to the routine where the restart originated. If the desired option is present, the pointer parameter is used to dispatch to the required routine in the option. For example, RST 2 OCT 2 calls the routine specified by the third location in the dispatch table located near the beginning of the HP-IB ROM (the table starts with location 0). RST 2 OCT 2 is executed during the 1980A/B main loop. This entry lets the HP-IB take control of the 1980A/B if the HP-IB controller sends a message or if the controller wants the 1980A/B to talk.

The entries in the dispatch table are as follows (these restart links are general-purpose and apply to all interface types):

0 Initialize at power-up
1 Entry for softkey menus
2 Main parse and talk entry
3 Service request invocation
4 Interrupt service
5 Return to local.

Another link table located just after this dispatch table is included so that features such as the plug-in can reach the bus without having to duplicate the HP-IB code. These links help the HP-IB ROM take care of the housekeeping necessary to run the bus activities properly.

Controlling the 1980A/B Hardware

Control of the hardware falls into three major categories—control of rotary control functions, control of state functions, and control through key closure.

An area of the 1980A/B's nonvolatile RAM contains the information that describes the mainframe's condition. By modifying specific RAM locations and calling the proper setup routines, the HP-IB can change the state of the 1980A/B hardware.

For the rotary control functions, the HP-IB places the desired value (e.g., a sweep speed) in the RAM locations that describe the function to be changed. A dispatch routine located in the mainframe is called and selects the rotary control slew routine for the selected function. In this case the HP-IB sets a status flag that tells the slew routine not to monitor the rotary control but to set up the 1980A/B according to the value in RAM and return to the HP-IB.

Control of state functions is similar. The RAM is modified to reflect the new state, and mainframe routines are called to handle the desired functions. The major difference is that new state changes are not output to the hardware immediately, as for rotary control functions. State function changes set a flag that determines the hardware setup necessary, and these flags are collected until a line feed is detected in the incoming message. At that time, the proper hardware output routines are called. This eliminates multiple calls to the hardware output routines when a command message changes more than one system state. It also increases programming speed.

For key closure control, the HP-IB simulates the operation of the front panel and makes the 1980A/B perform as if a front-panel key had been pressed. This is a secondary mode of programming and is included so that menus can be accessed from the HP-IB. The programmer can do almost all remote programming via key closure, but this type of programming won't run as fast as direct programming.

Interface Operation

Listening on the HP-IB is done under a simulated interrupt system. Rather than have each incoming character generate an interrupt, the first character generates the interrupt and the rest of the message is received by polling the HP-IB talker-listener IC. As long as characters come quickly, the 8085 microprocessor remains in the interrupt service routine. If the characters don't come quickly enough, as in the case of a slow controller, the interrupt service routine saves its state and returns. When the next character comes in, another interrupt is generated and the interrupt service routine continues where it left off.

Characters are placed in a buffer as they are received. When a line feed is received, remote-local status and buffer overflow are checked. If everything checks out, a flag is set so that the next time the HP-IB is polled from the 1980A/B main loop, the command in the buffer will be parsed and executed. Commands are executed by polling from the main loop so that the HP-IB does not make any changes while the 1980A/B is doing something else, such as an Autoscope.

Talking, like command execution, is done by polling from the main loop. When polled, the HP-IB code checks to see if the 1980A/B is addressed to talk. If so, the HP-IB verifies that it has been told what to say by a previously executed output command and outputs the proper information. The HP-IB interface must always be told what to say before it is asked to say it. An unspecified request to talk results in the output of E CRLF.

There are seven conditions that generate service requests, and they are individually maskable (see Fig. 2). When all conditions are masked, a single byte is available during a

Program Code	Function
AC <mode>	Vertical Mode (alt-chop select)
AS	Autoscope
AV <state>	Advisory Messages on/off
BA <state>	HP-IB Status Advisory on/off
BW <state>	Bandwidth Limit on/off
CG <state>	Character Generator on/off
CI <value 1> [,<value 2>]	Intensity, Trace
CH <line #>[,<string>]	Text Display (with attributes)
CL <mode>	Calibrator Level
DD <value>	Delay (digital delay)
DG	Waveform Storage
DL <value>	Trigger, Delayed Sweep (level)
DM <mode>	Sweep Mode, Delayed
DS <value>	Sweep Speed, Delayed
DT[<slope>]<source>,<coupling>	Trigger, Delayed Sweep
DV <channel>, <state>	Delta Volts on/off
DY <value>	Delay (delay time)
DZ <state>	Delta Time on/off
FP <char>[,<lamps>]	Intensity, Readout
HM <mode>	Horizontal Mode
HP <value>	Horizontal Position
IM <value>	SRQ Condition (RQS mask)
IN	Initialize
KY <code>[,<code>]...	Key Press
ML <value>	Trigger, Main Sweep (level)
MS <value>	Sweep Speed, Main
MM <mode>	Sweep Mode, Main
MT[<slope>]<source>,<coupling>	Trigger, Main Sweep
OF <code>	Reading Values (output function)
OQ <code>	Instrument Status (output qualifier)
P	Plug-In Expansion Module
Q	Feature ROM
RC <code>[,<step>]	Control Knob
SA	Autoscope (selective)
SG	Trigger Flag (initialize flag)
SK <code>[,<code>]...	Softkey Press
SM <mode>	Scope Mode
SP <value>	Separation, Dual
SW <value 1>,<value 2>,<value 3>	Trigger Flag (sweep wait time)
TE	Learn Mode (output learn string)
TF <mode>	Trigger Flag
TV <mode>	Trigger View
TX <line #>[, <string>]	Text Display
VC <channel>, <mode>	Vertical Coupling
VM <mode>	Vertical Mode
VP <channel>, <value>	Vertical Position
VS <channel>,[<polarity>]<value>	Vertical Deflection Factor

Fig. 3. *1980A/B HP-IB instruction set.*

```
0: "Find Vertical Routine":
1: "1980A/B Address is 707":
2: "This routine duplicates the Autoscope Vertical Find":
3: "on Channel 1":
4:
5: wrt 707,"in;ml150;ma5.00e-9;da5.00e-3;hm3;cg0;vm1;pm0;im4"
6: wrt 707,"vp1.0;sw242,8,0;tf3;rc1"
7:
8: fmt 1,"va1,",f3.0,"e",f2.0
9: fmt 2,"ml",f4.0
10: 100-V;-2-R;150-L
11:
12: "V1":
13: wrt 707,1,V,R
14: gsb "signal"
15: if A=1;gto "V6"
16: gsb "swapTL"
17: gsb "signal"
18: if A=1;gto "V6"
19: R-1-R
20: if R>-5;gto "V1"
21: if R=-5;200-V;gto "V1"
22:
23: "V5":
24: wrt 707,"va1,2.00e0;cg1;tx5,NO SIGNAL FOUND"
25: wait 2000
26: wrt 707,"tx"
27: gto "end"
28:
29: "V6":
30: V+100-V
31: if V>900;900-V;gto "V8"
32: wrt 707,1,V,R
33: gsb "signal"
34: if A=1;gto "V6"
35: gsb "swapTL"
36: gsb "signal"
37: if A=1;gto "V6"
38: gsb "swapTL"
39: V-100-V-S
40:
41: "V8":
42: V+10-V
43: if V-S>90;gto "V9"
44: wrt 707,1,V,R
45: gsb "signal"
46: if A=1;gto "V8"
47: V-10-V
48: wrt 707,1,V,R
49:
50: "V9":
51: wrt 707,"cg1"
52:
53: "end":
54: wrt 707,"em1;im0";lcl 707;cli 7
55: end
56:
57:
58: "signal":
59: wrt 707,"sg"
60: if bit(7,rds(7))=0;jmp 0
61: rds(707)-B;wrt 707,"oq3";red 707,A
62: ret
63:
64: "swapTL":
65: -L-L;wrt 707,2,L
66: ret
67:
68: end
```

Fig. 4. *The 1980A/B's trigger flag lets the user write custom routines like this one for an HP 9825A Desktop Computer. The routine simulates part of the 1980A/B's Autoscope algorithm. Lines 5-6: Preset the 1980, set trigger flag to latch on main trigger event and wait 40 ms for trigger. 8-9: Format statements for channel 1 vertical sensitivity and main trigger level. 10: Set sensitivity mantissa and exponent and main trigger level. 12-21: Set sensitivity, least sensitive range first. If no signal is found on a range, swap the trigger level sign. If signal is still not found, go to next sensitive range. Line 21 takes care of special case on most sensitive range. When signal is found, go to line 29 with proper range set. 23-27: Display "No Signal Found." 29-37: Decrease sensitivity by increasing mantissa's most significant digit until signal is lost. If signal is lost, change sign of trigger level and try again. 38-39: When signal is lost, swap the trigger level and set the mantissa back to where the signal was last found. 41-46: Decrease sensitivity by increasing mantissa's middle digit until signal is lost. 47-48: Decrease mantissa middle digit to where signal was last found. 50-55: Turn the character generator back on and put the 1980A/B in LOCAL. End of Find Vertical. 58-62: Signal subroutine arms the sweep and returns with a triggered or no-triggered flag in variable 'A'. 64-66: Trigger level swap changes the sign of the main trigger level.*

serial poll that indicates which conditions have occurred since the status byte was last cleared.

When one or more conditions are unmasked, as many as nine separate service requests can be queued in a status byte stack. The stack is organized as a FIFO (first-in, first-out) memory and is read by serially polling the 1980A/B. If more than nine service requests are generated before a serial poll, the stack will contain the status byte for the first eight and the last service requests. The status byte and the stack are initialized and cleared at power-up, when a new mask is specified, and when the HP-IB address mode menu is selected.

The 1980A/B implements the complete remote-local state diagram of IEEE 488. This means that remote and local modes, with and without local lockout, are available. When the 1980A/B makes a local-to-remote transition, the front-panel keys are disabled and the control knob is put in HOLD. The controller can re-enable control knob functions as desired and the user can write programs to enable particular keys. The controller may redefine these keys, since keys pressed while in REMOTE signal the controller but do not

cause execution of the function. The controller can decide how to act when a key is pressed and can issue the appropriate commands to the 1980A/B.

Instruction Set

The HP-IB instruction set, outlined in Fig. 3, completely controls all front-panel features and supplies access to the waveform storage, expansion module, and feature ROMs. It also controls the trigger flag, which is not directly accessible from the front panel.

The trigger flag is a feedback line from the analog hardware to the 8085 microprocessor. Simply stated, the trigger flag lets the microprocessor know if a trigger event occurred during the delayed sweep time. The 1980A/B mainframe uses the trigger flag to implement the Autoscope algorithm. The HP-IB user has access to the trigger flag with the TF, SW, and SG commands. The trigger flag lets the HP-IB user write custom AUTO routines. Fig. 4 is a 9825A Computer/Controller listing of a routine that simulates the vertical find section of Autoscope.

Control of Plug-in Options

The plug-in expansion module, waveform storage, and feature ROMs do their own instruction parsing, instruction execution, and talking. If a P is detected in the command string, the HP-IB restarts to the expansion module so that the module can decode the rest of the message. The expansion module can use HP-IB parsing subroutines to decode messages it may receive. If the controller wants the expansion module to talk on the bus, the module sets a flag in RAM that tells the HP-IB to restart to the module the next time the 1980A/B is addressed to talk. The module then uses the HP-IB talk capabilities to put its message on the bus.

The DG command for the waveform storage option and the Q command for the feature ROMs operate like the P command.

Acknowledgments

I would like to thank Dana Johnson for his great help in debugging the code and Paul Austgen for giving me the opportunity to work on the HP-IB interface and being a terrific sounding board when the problems seemed insurmountable. Special thanks go to Don Loughry for the countless hours spent on the telephone helping me to understand the intricacies of the HP-IB.

Michael J. Karin

Mike Karin received his BSEE degree from the Georgia Institute of Technology and joined Hewlett-Packard's Colorado Springs Division in 1973. He spent several years designing and programming computer-based test systems and a year in factory marketing before joining the 1980A/B R&D project. He developed HP-IB hardware and software for the 1980A/B and was project leader for the 19860A Waveform Storage option. A resident of Colorado Springs, Colorado, Mike is married, has two children, and enjoys running, swimming, and downhill skiing.

Mechanical Design of the Oscilloscope Measurement System

by John W. Campbell

THE MECHANICAL DESIGN of the 1980A/B Oscilloscope Measurement System contributed to the circuit development and performance as well as to the producibility, serviceability, and versatility of the product.

Mechanical design in the electronics industry is often focused on such parameters as thermal performance, circuit area, volume and support, cost control, and the development of special functions. Often, designing around the circuits is the main thrust of a design.

The 1980A/B product definition presented particularly difficult design challenges. To meet them meant approaching the task of mechanical design from a different angle and with a different basis. Because of the digital/analog complexity of the product, mechanical design became an important foundation for the circuit development process.

Rack and Stack Configurations

It was determined that the product would be developed in two configurations: a 425×133-mm rack version for system applications and a 213×267-mm bench style (Fig. 1). The primary design objective was to make the two units as similar as possible—to strive to have one set of components for two models. This would minimize the development cycle required for two units. To meet this objective, two initial design goals were set:

- The circuits, internal interfaces, grounding, and coupling for the two models were to be as similar as possible.
- Because of circuit complexity, the products had to be simple to produce and service.

The list of potential configurations for such a system was extensive. The first and most obvious solution was to build

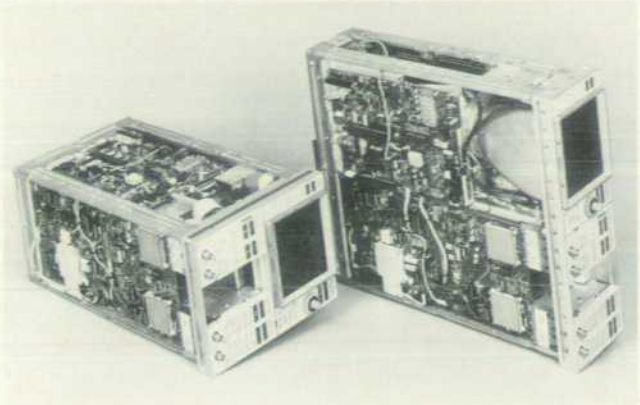

Fig. 1. *Models 1980A (left) and 1980B are designed to have as many components and boards in common as possible.*

a top-and-left module and a bottom-and-right module. There were, however, major drawbacks with this approach. The interfaces were not identical, circuit board size was restricted, and serviceability was severely impaired. The same problems, plus additional packaging costs, came up when a similar solution was considered. This approach used boxes of circuits: power supply, vertical, horizontal, and display. Ultimately, a modified modular approach on an appropriate level of implementation was decided upon (Fig. 2).

Modular Approach

The modular approach consists of modules small enough to effect the same interface and coupling interrelationships in both configurations. For example, the low-voltage-supply printed circuit board, filter capacitors, line transformer, heat sink, and chassis-mounted rectifiers could not have had the same interface relationships in both units had these components been built into a power supply module. To make the common-relationships concept effective, it was necessary to consider not only board shape but circuit locations within the boundaries of the board. As a result, all interconnecting cables, except for four non-signal-path cables, are the same length. Four large circuit boards are the basic modules, providing a logical, comfortable, uncomplicated architecture. All the circuits are directly below the instrument covers, a feature that contributes significantly to the serviceability of the 1980A/B. The circuit boards surround the CRT display, power supply transformer, filter capacitors, some supply chassis components, attenuators, and the enhancement module port. The CRT display assembly, vertical and trigger attenuators, four front panels, and rear-panel heat-sink/fan assembly are all modular. There is also a rear input/output panel and battery module.

The mechanical structure keeps interrelationships between circuits electrically as similar as possible between the two configurations. For example, if a board has a deck under it in one model, it has one in the other model as well. In both configurations, the enhancement module makes its sync line interconnection directly in the midst of the vertical and trigger circuits. In both configurations, the vertical deflection amplifier, part of one of the four big boards, has the same relationship to and distance from the CRT, but with a 90° plane change.

Configuration-Controlled Interface

Only one of the circuit boards varies between the two models. To fit the different configurations, the interface boards could not be identical. Each interface board makes 266 connections and is the power supply and processor bus distributor for all the major boards. It is also the interconnection for the enhancement modules. Although it is buried in the instrument, it contains no components. But because it carries digital and analog lines, some development was necessary. Once established, the interrelationships of the digital, power supply, and signal lines are permanent. This would not have been possible if a laced cable, which would have required about 140 wires, had been used instead. The cable would have represented a constantly variable coupling situation.

An Old Problem

While tackling the new design problems of the 1980A/B, an attempt was made to solve an old problem as well. Traditionally, CRT mounting and graticule alignment are sore points during instrument assembly because of conflicting requirements. Providing a relatively stiff shock mounting in the front that can accommodate a range of faceplate glass sizes can conflict with allowing for rotational adjustment of the glass for positioning the graticule squarely with the structure.

Typically, a mounting system consists of elastomer pads or wraps applied to the supporting structure or the glass. When combined, the dimensional tolerances on the elastomer parts and glass sizes produce a mounting either too soft or too stiff to allow rotational adjustment. Even if rotational adjustment is possible, the CRT cannot be in equilibrium and may snap back out of alignment by slipping in its rotational clamping device. To solve the mounting problems and to avoid the awkward adjusting and tightening of devices within the instrument, the 1980A/B approach includes two major departures from typical designs. First, the CRT assembly, including front-end mount, shield, tube, and shock mounting, is assembled and aligned outside the

Fig. 2. *Modular design approach results in modules small enough to have the same interface and coupling relationships in both configurations. Only one circuit board, the interface board, differs between the two 1980A/B models.*

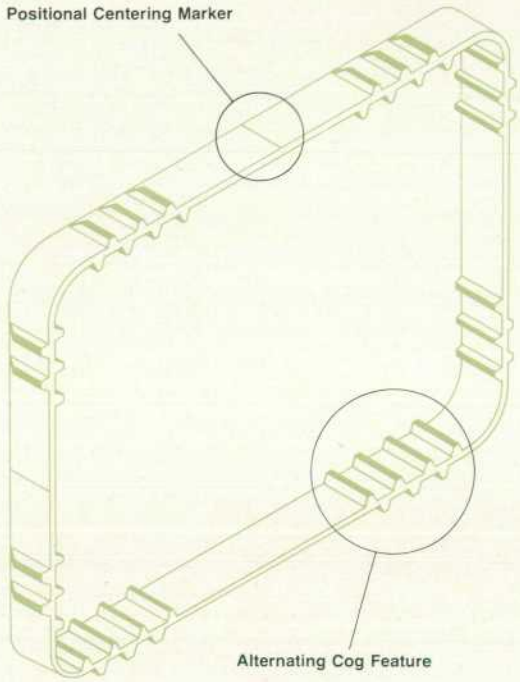

Fig. 3. *Injection-molded elastomer belt for shock-mounting and alignment of 1980A/B CRT.*

instrument. Second, an injection-molded elastomer belt (Fig. 3) solved the shock-mounting and alignment problems. The belt serves as a shock mount that adapts to different glass sizes. It does this via flexure of the belt within the areas of the alternating cog features. It is also a positive-displacement rotational adjustment device which leaves the CRT in rotational equilibrium regardless of adjustment position. The belt takes advantage of the curvature of the sides of the glass faceplate. As an illustration, a perfectly symmetrical tube with properly aligned graticule is shown in Fig. 4a. With the belt centered on the glass, the graticule is aligned horizontally and vertically. By rotating the belt in one direction (Fig. 4b), the glass is rotated in the opposite direction and remains in equilibrium because the mounting cogs attempt to fill and then relieve the voids left by the glass curvature on each side.

Acknowledgments

I would like to acknowledge the efforts of the other members of the mechanical design group that developed the 1980A/B package: Donna Burton, now a graphic artist, for persevering with the drafting, redrafting, checking and analyzing the drawings, Ernie Hastings, who finalized the structural parts designs and carried the cabinet model into production, Will Taylor for all of the many designs he contributed in addition to the attenuator design, Jim Carner, now a process manufacturing engineer, for the initial enhancement module design, and Carolyn Finch for the panel assembly design.

John W. Campbell

John Campbell, who has been with Hewlett-Packard since 1972, worked on the 1740A Oscilloscope before becoming mechanical design project leader for the 1980A/B System. Before joining Hewlett-Packard, John spent four years as a space systems analyst in the Air Force. He received a BS degree in applied engineering in 1967 and an MS in industrial management in 1968, both from Bradley University in Peoria, Illinois. John is married, has two sons, and lives in Colorado Springs. He enjoys skiing, dirt biking, and golfing, but his primary hobby is model railroading.

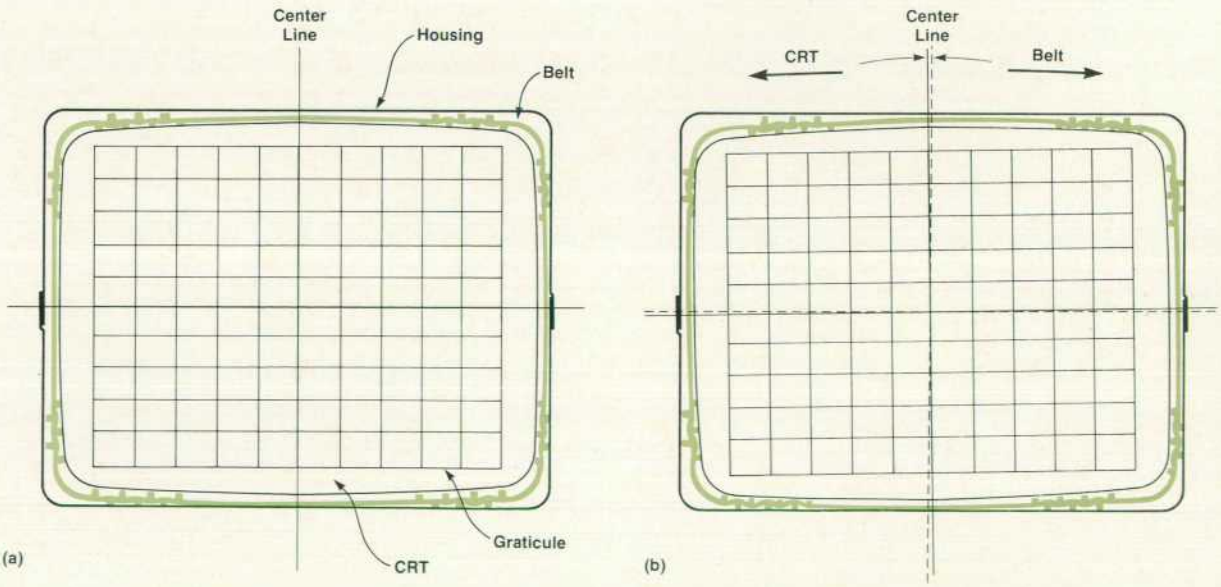

Fig. 4. *(a) Symmetrical CRT with properly aligned graticule. (b) With elastomer belt rotated in one direction, the glass tube is rotated in the other direction but remains in equilibrium.*

A High-Performance Bipolar Integrated Circuit Process

Ion-implanted collector, base, and emitter regions in an oxide-isolated structure result in compact high-performance bipolar transistors with reduced power consumption for use in high-density integrated circuits.

by Irene V. Pecenco and Albert S. Wang

TODAY A NEED EXISTS within Hewlett-Packard for high-speed, high-density integrated circuits that are easily designed and can be fabricated quickly. To supply this need, a new high-performance bipolar process was developed at HP's IC Division in Santa Clara, California. The process is capable of producing parts for high-speed amplifiers, counters, analog-to-digital converters, and semicustom logic applications where emitter-coupled logic (ECL) circuitry is expected to perform at clock rates greater than 1.25 GHz. In addition to speed and density, another process objective was the reduction of power consumption by horizontally scaling down device size.

Process consistency and manufacturing ease are also part of the development goals. The active portions of the transistor, that is, the emitter, base, and collector, are implanted to optimize performance yield and process control. The advantages of dielectric isolation are fully used to simplify fabrication.

Since metallization holds the key to the success of a bipolar process, both in density and yield, emphasis was placed upon developing a reliable multilevel metallization technique. Special attention was also given to the circuit layout design rules so that any improvements in the technologies can be transferred directly to existing designs without having to lay out the circuit again. For example, a direct shrink of the chip size should be easily realized. Thus, a close association was sought between process and design-aid development so that a complete package can be offered to the user.

Device Design

With advances in process techniques such as dry etching and projection photolithography, significant reductions in device dimensions and metal linewidths can be achieved. These improvements not only increase the component packing density of an integrated circuit, but also enhance device performance. The general design goal of a high-performance bipolar npn transistor is to achieve subnanosecond gate delay and short access time. Some of the design features of HP's high-performance bipolar process can be summarized as follows (see Fig. 1):

- Collector/epi: To minimize collector series resistance, a heavily implanted arsenic subcollector coupled with a collector-wall connection is used. To further reduce series resistance and collector transit time, a thin, n-type

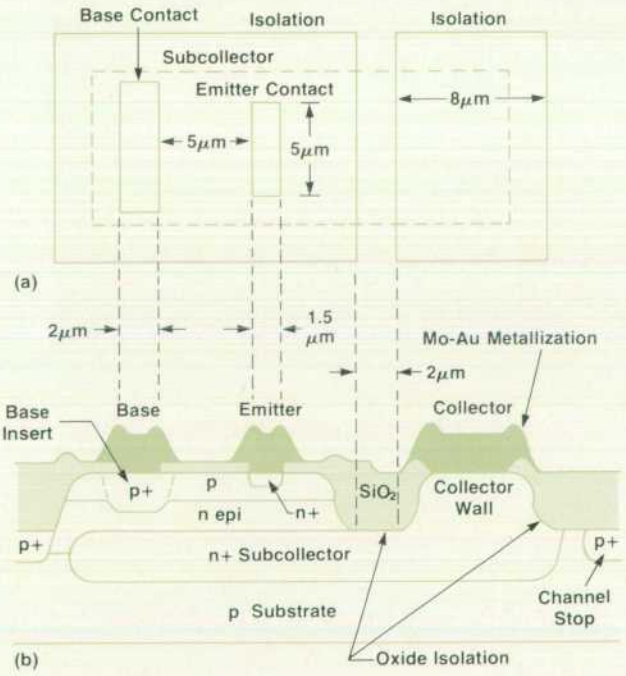

Fig. 1. *(a) Top (mask design layout) and (b) cross-sectional (physical structure) views of a typical bipolar transistor for the high-performance bipolar process.*

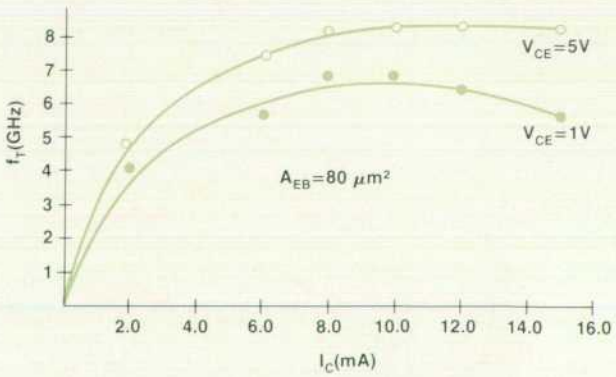

Fig. 2. *Bipolar transistor f_T performance as a function of collector current and collector-to-emitter voltage.*

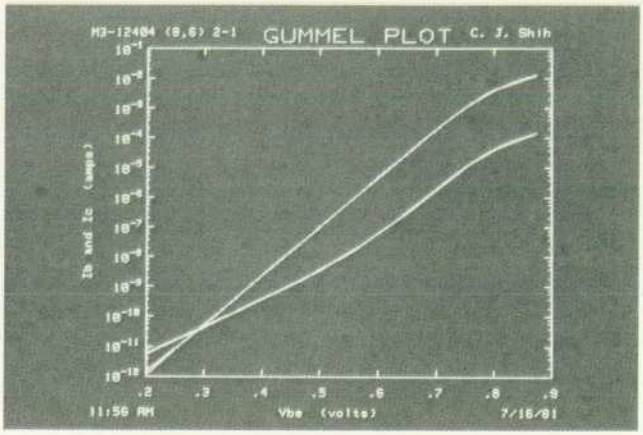

Fig. 3. *ac bias dependence of bipolar device characteristics.*

epitaxial layer is grown just thick enough to sustain the required breakdown voltage.

- Isolation: Oxide isolation is used for several reasons: higher component packing density, lower parasitic device capacitance, and reduced alignment criticality for mask layers where overlap onto the field oxide can occur. The thick isolation oxide, coupled with reduced metal linewidths, also reduces parasitic line capacitance.
- Base/emitter: For high f_T, a narrow boron-implanted base with a shallow arsenic-implanted emitter was developed without sacrificing yield. To reduce base resistance and operating power, a narrow (1.5-μm) emitter is opened by 10:1 projection photolithography. A base-insert step is also added to minimize base contact resistance and extrinsic base resistance.
- Metallization: A composite layer of molybdenum and gold is used to allow reduced metal linewidths while retaining a high resistance to electromigration failures.
- Miscellaneous devices: pnp transistors can be fabricated by using the relatively deep base-insert junction. Schottky diodes can be made by using the molybdenum metallization. Low-value resistors fabricated by using the base-insert implant and relatively high-value resistors using the base implant are recommended for the process.

Table I
Typical SPICE Parameters for High-Performance Bipolar Process

Parameter	Units
J_S (saturation current) $=4\times10^{-17}$	A
β_F (forward beta) = 135	
R_B (base resistance) = 175	Ω
R_E (emitter contact resistance) = 7	Ω
V_F (forward Early voltage) = 30	V
C_{je} (emitter junction capacitance) = 0.06	pF
C_{jc} (collector junction capacitance) = 0.19	pF
t_F (forward transit time) = 19	ps

The performance of a device design is usually measured by its parameters used in the SPICE circuit analysis program developed by the University of California at Berkeley. To demonstrate performance, Table I gives a list of some of the key parameters measured.

Since device performance is primarily related to the operating conditions, Fig. 2 and Fig. 3 illustrate the dc and ac bias dependence, respectively.

Device Fabrication

The size of the minimum-geometry bipolar transistor shown in Fig. 1 is approximately 700 μm^2. This device is fabricated in an eleven-mask process that uses dual-layer metallization for flexibility of device interconnection. The process was chosen to maximize device performance and

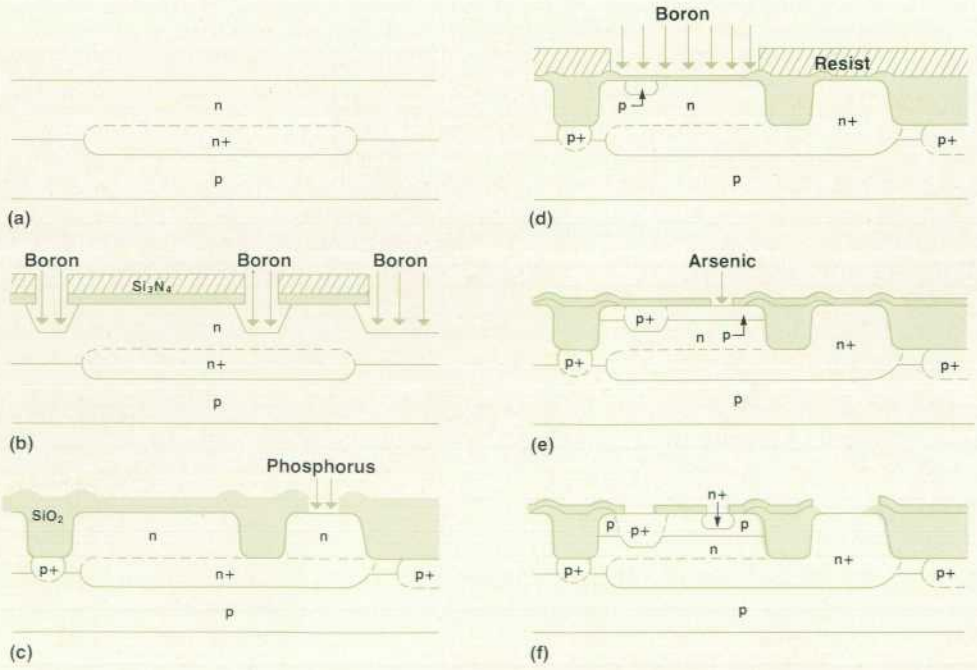

Fig. 4. *Simplified process sequence for fabricating high-performance bipolar devices. (a) Growth of epitaxial layer after buried layer diffusion. (b) Isolation pattern is defined and after plasma etching the exposed silicon, the channel stop is doped. (c) After the isolation oxidation, the collector wall is defined and doped. Then the base insert is diffused. (d) After a short oxidation cycle, resist is used to mask the base implant. (e) A layer of silox is deposited and patterned for the arsenic emitter implant. (f) Contact openings are defined. The cross section after the next step, first-layer metallization, is shown in Fig. 1b.*

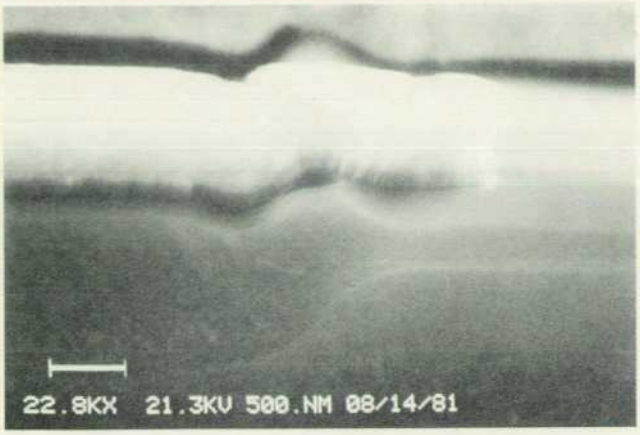

Fig. 5. *Cross section of an oxide isolated structure.*

density while maintaining good producibility in a manufacturing environment. A simplified process flow is shown in Fig. 4.

The oxide isolation is achieved by the standard technique of depositing and then defining a silicon-nitride mask over the active device areas. The exposed areas are plasma etched and a thin oxide is grown in these regions. A channel-stop mask is applied, and after a boron predeposition, the exposed areas are oxidized to a thickness of 1.2 μm. The depth of the plasma etch step removes enough silicon in the exposed areas so that the surface after oxidation is approximately planar. Fig. 5 shows an actual cross section of an oxide isolation structure. The boron channel-stop diffusion prevents the formation of a conduction channel between subcollectors that may occur from n-dopant accumulation and p-dopant depletion during oxidation.

The collector, base, and emitter are implanted for excellent control of device characteristics. Sheet resistances of implanted layers can be maintained to within 5% of target values. This ensures that the uniformity of transistor and resistor characteristics across a wafer, and from wafer to wafer, can be specified more exactly than has been previously possible. Another advantage is that photoresist can be used as an implantation mask, thus allowing for greater process flexibility because doped areas may be defined solely by a resist process. This eliminates the need for a sequence of oxidation and oxide-etching steps that makes it difficult to maintain good dimensional control.

Metallization often limits circuit density in bipolar designs. A dual-layer molybdenum-gold (Mo-Au) system is used in this process (see Fig. 6). The first metal layer is deposited as a composite Mo-Au-Mo film. The top layer of molybdenum is patterned by resist and plasma etched in a SF_6-based system. The patterned molybdenum serves as a mask for etching the underlying gold layer during the subsequent sputter etch step. The exposed molybdenum areas (both top and bottom films) are then plasma etched, leaving a Mo-Au film which replicates the original pattern with less than 0.2 μm undercut per side. A conventional CVD (chemical vapor deposition) oxide is used as the interlayer dielectric. The second layer metal deposition consists of a sputtered Mo-Au film. After patterning, the gold layer is electroplated to a thickness of 2.5 to 3 μm. This procedure ensures good step coverage over first-layer metal lines. This metallization process can easily achieve first-layer-metal and second-layer-metal pitches* of 5 to 6 μm and 10 to 11 μm, respectively.

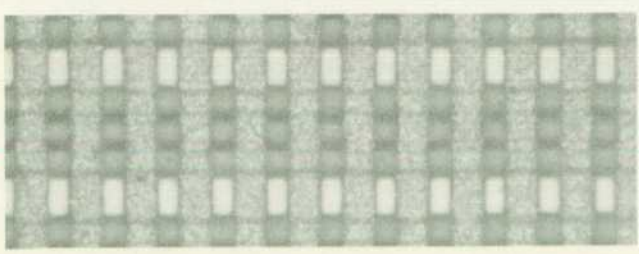

Fig. 6. *Top view of the dual-layer metallization.*

The design rules for this process are based on the use of a direct-step-on-wafer (DSW) projection system with a positive photoresist process. The minimum feature size is a 1.5-μm-wide emitter stripe and alignment tolerances are approximately 1 μm.

Acknowledgments

The development of the high-performance bipolar process depended on the collected results of work done by many people at several divisions of Hewlett-Packard. Their contributions are greatly appreciated.

*Pitch is the distance between the centerlines of adjacent metal lines in a periodic pattern of lines separated by equal-width spaces.

Albert S. Wang

Al Wang joined HP in 1969 as a development engineer. He left in 1972 to complete his studies at Stanford University and was awarded the PhD degree in electrical engineering in 1975. Al returned to HP in 1974 and has progressed from being a project manager in HP Laboratories to his current position as wafer fab manager at HP's Santa Clara Division. He has written a few papers on electron devices, is a member of the IEEE, and has taught semiconductor devices for the University of California at Berkeley Extension. Born in Chungking, China, Al is married and has two daughters. He lives in Palo Alto, California and enjoys the outdoors.

Irene V. Pecenco

Irene Pecenco was born in Scheveningen, The Netherlands, and attended the State University of New York at Buffalo, earning a BSEE in 1976, and Stanford University, earning an MSEE degree in 1977. She then joined HP as a development engineer doing IC research and development. Irene currently is both an R&D section manager and a production process engineering manager at HP's Santa Clara Division. She is married, lives in San Jose, California, and enjoys swimming and playing tennis.

Synthesizer Accuracy for Unsynthesized Microwave Sources

This source synchronizer stabilizes microwave sources to provide accurate continuous-wave or swept-frequency outputs. It also provides a high-performance microwave counter.

by V. Alan Barber

GENERAL-PURPOSE MICROWAVE signal sources in use today can be classified into three broad categories. In wide use are signal generators, which are manually tuned instruments generally offering versatile modulation capabilities, reasonably low phase noise and low frequency drift over frequency ranges of an octave or more at an attractive price. The klystron oscillators of the past are being replaced by GaAs FET oscillators in modern instruments.[1] These generators are particularly useful for signal simulation in receiver testing, especially when combined with a frequency counter for accurate frequency setting.

The second category is sweep oscillators. These versatile instruments offer broadband sweep operation over more than three decades. Programmability makes these units particularly suited to component measurement applications, especially in automatic systems. Again, the frequency accuracy needs of a system may require the use of an external frequency counter. Modern sweep oscillators are commonly made with GaAs FET or Gunn devices, are YIG-tuned and are often combined with frequency multipliers for higher-frequency operation.

The third category is synthesizers. These generators offer the ultimate in frequency accuracy and phase-noise performance. The best of them offer some of the features of signal generators, such as versatile modulation and calibrated power output. These find broad application in signal simulation and automatic test systems.

With the new 5344S Source Synchronizer, Fig. 1, the owner of a signal generator or sweeper can give it the superior frequency accuracy of the synthesizer and add some new capabilities never before available in a general-purpose microwave signal source. A sample of the signal to be stabilized is sent to the 5344S, and for CW operation, the desired frequency is entered on the 5344S front panel. The sample signal is down-converted to an intermediate frequency and compared with an internal crystal-controlled synthesizer, and a correction voltage is developed and applied to the frequency modulation port of the signal source. The source may be phase-locked in this manner at any frequency in 1-Hz increments from 0.5 to 18.0 GHz (26.5 GHz optionally), with accuracy and long-term stability equal to that of the reference oscillator in the 5344S.

In addition to simple CW synchronization, the 5344S provides two highly accurate sweep modes of operation. For narrowband sweeps (up to 40 MHz wide), the 5344S provides a phase-locked, phase-continuous sweep. The signal source operates in the CW mode with the 5344S forcing the sweep with a ramp voltage to the source's FM input. Thus a signal generator can become a sweeper, at least over narrow bandwidths. Furthermore, since the sweep is always phase-locked, it has synthesizer precision throughout its range, and there are no phase transients as the frequency is swept. Up to four markers, again with synthesizer precision, are available for use in the traditional way.

Broader phase-locked sweeps are not possible because of the limited IF bandwidth of the synchronizer, but the 5344S

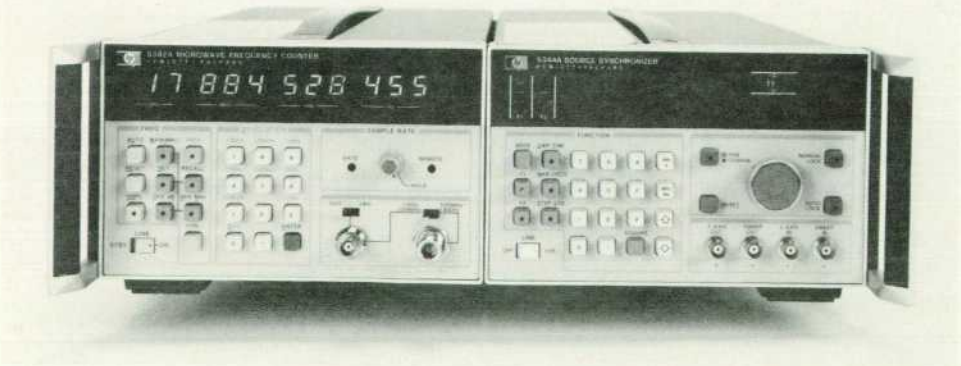

Fig. 1. *The HP 5344S Source Synchronizer System consists of the 5344A Synchronizer and a microwave counter. With the 5342A Counter, the 5344S operates to 18 GHz. With the 5343A (Option 043) it operates to 26.5 GHz.*

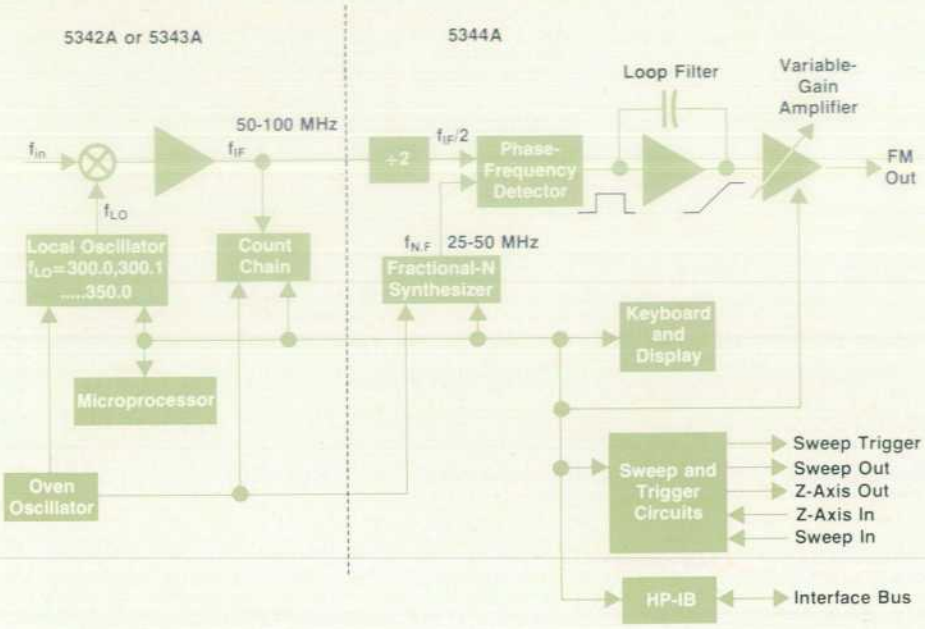

Fig. 2. *5344S Source Synchronizer block diagram. For frequency control of the source being stabilized, the FM output of the 5344S is applied to the source's FM input.*

can dramatically improve the accuracy of broadband sweeps in a mode we call "lock and roll." Here the user sets up a normal sweep on the sweep oscillator, say from 2 to 3 GHz, then enters the start frequency on the 5344S (with 1-Hz resolution). The source synchronizer momentarily phase-locks the sweeper at 2 GHz for each sweep. The resulting correction voltage is held at the FM input and the sweeper is triggered to make the sweep in the normal fashion. What this accomplishes is much improved accuracy (typically 50 kHz) at the start frequency and the removal of frequency offset errors, the largest error contributor, from the rest of the sweep. In addition, with Option 043 and the HP 8350A Sweep Oscillator as the sweeper,[2] marker and stop frequencies can be measured dynamically with the counter during a measurement, allowing for easy manual adjustment of these frequencies.

The sample signal for phase-locking the 5344S may be obtained from a directional coupler or power splitter on the output of the signal source. However, many sources, including all HP broadband sweeper plug-ins and 8683A and 8684A Signal Generators, provide an auxiliary output. This output may be a subharmonic of the regular output frequency or offset from it. The 5344S can automatically determine the subharmonic multiple and apply it appropriately before phase-locking. It can also apply a user-entered offset to the phase-lock frequency. Since the 5344S is capable of 0.02-Hz resolution internally, the resolution of 1 Hz on the output frequency is maintained even when using an auxiliary output at the fiftieth subharmonic.

In manual operation it is necessary to tune the source within 25 MHz of the desired frequency, but if the source is an HP Model 8620C Option 011 or 8350A Sweeper, then the 5344S performs this task automatically. In AUTO LOCK mode the 5344S becomes an HP-IB* controller and can set the frequency and mode of the source using one additional interface cable. This makes operation extremely simple; the user only needs to enter the desired frequency on the 5344S front panel or adjust it using the control knob or step keys.

*HP-IB is Hewlett-Packard's implementation of IEEE Standard 488 (1978).

System Organization

Fig. 2 shows the basic architecture of the 5344S. This system is a combination of a 5342A Microwave Frequency Counter (optionally a 5343A) and the new 5344A; thus the S in the model number refers to the combined system. The frequency counter alone performs its function by mixing

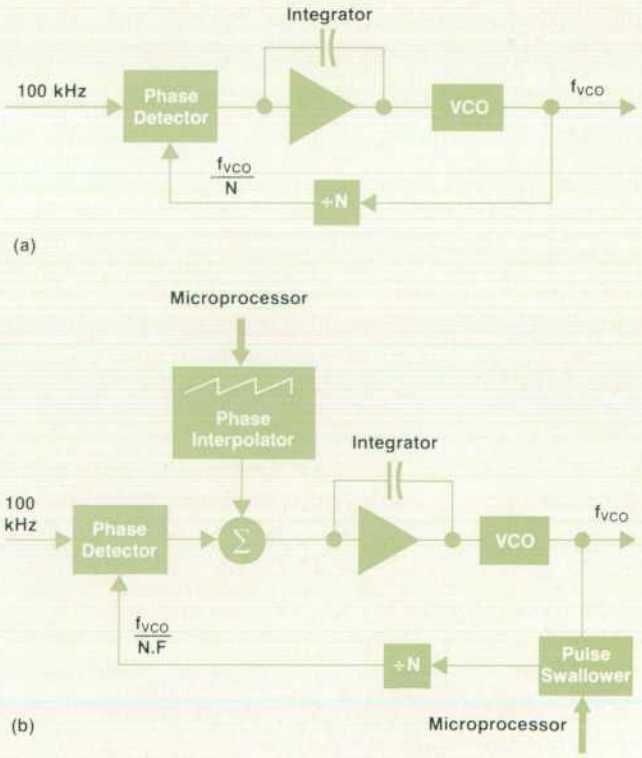

Fig. 3. *(a) Traditional divide-by-N synthesizer. (b) Fractional-N synthesizer.*

the unknown input signal f_{in} against the Nth harmonic of a precisely synthesized local oscillator f_{LO}, then counting the lower intermediate frequency f_{IF}. The input frequency is then calculated from:

$$f_{in} = Nf_{LO} \pm f_{IF} \quad (1)$$

and displayed.[3]

Conceptually this process can be reversed. If we know what we want the input frequency f_{in} to be, we can force N, f_{LO}, the sideband (+ or −), and f_{IF} to values that satisfy equation 1 and the result must be the frequency we desire. This is the task performed by the 5344S.

To understand how this is done, consider the example of a user who wishes to stabilize a sweeper at 10575.000000 MHz. A sample of the sweeper output is sent to the 5344S input (f_{in} in Fig. 2) and the FM output is connected to the sweeper's FM input. The desired frequency is keyed into the 5344S and from that the appropriate values of N, f_{LO}, the sideband, and f_{IF} are calculated. N must be an integer between 2 and 88. The local oscillator frequency f_{LO} must be between 300.0 and 350.0 MHz in steps of 0.1 MHz. The intermediate frequency f_{IF} may be between 50 and 100 MHz with a resolution of 0.02 Hz. For this case the following values would be chosen:

f_{in}	= 10575.000000 MHz
N	= 30
f_{LO}	= 350.0 MHz
sideband	= +
f_{IF}	= 75.00000000 MHz

The system guarantees that the correct N (30) and sideband (+) are used by checking that the free-running source frequency is close enough to the desired frequency so that it will produce an IF (25-125 MHz) only when heterodyned on the upper sideband of the 30th harmonic of 350 MHz. Then the local oscillator will be set to 350 MHz and the fractional-N synthesizer set to 37.5 MHz, or one-half of f_{IF} because the IF is divided by two before the phase detector. The phase/frequency detector produces the dc voltage necessary to adjust the frequency of the microwave source until $f_{IF}/2$ is in phase with and therefore equal in frequency to $f_{N.F}$, the output of the fractional-N synthesizer. If this is so, equation 1 is satisfied and phase lock is achieved at 10575.000000 MHz.

Although they are built separately, the 5342A and 5344A are connected both mechanically and electrically and operate as a single instrument, the 5344S. Two coaxial connections allow the instruments to share the IF signal and 10-MHz reference (a precision oven oscillator is standard in the 5344S). Between the instruments is a 40-pin ribbon cable carrying all the data and control lines from the microprocessor. The processor resides in the 5342A but program ROM and RAM are located in both instruments with control passed back and forth as necessary. With only the counter turned on, or with both instruments on but not in lock mode, the counter has control and operates in its normal way. While the system is locking a source, the synchronizer program has control and the counter cannot be used for other purposes. In the CW mode the counter continuously measures the synchronized frequency.

The key to the fine resolution and sweep capability of the 5344S lies in the fractional-N synthesizer.[4] This circuit provides the reference signal that the phase detector compares with the IF from the counter (divided by two). The synthesizer, to be described in the next section, is capable of 10-nanohertz resolution from 25 to 50 MHz, although it is used to only 10-millihertz resolution here. Its output frequency may be swept across its full range while phase-locked. As this frequency, $f_{N.F}$, is swept (see Fig. 2), the phase detector applies a correction voltage to the source in an attempt to force it to follow in frequency and keep the phase error at zero. Since the loop bandwidth is wide compared to the frequency components of the sweep ramp, the loop succeeds, as shown by the waveforms in Fig. 2. The output of the loop filter is a voltage ramp which causes the source frequency to ramp up. Since the loop filter is an integrator, its input is a voltage step, constant during the sweep and returning to zero at the end of the sweep. Thus, there is an offset in phase which is constant during the sweep. The phase detector is also an integrator, acting upon the frequency difference of the inputs, so frequency error is the derivative of the phase detector output. Thus, the frequency error during a sweep is nominally zero except for the brief (10-20 microseconds) transient at the beginning necessary to establish the phase offset (thirty degrees maximum) that drives the loop during the sweep, and a similar but opposite transient after the sweep ends. The result is that the precision and linearity of the low-

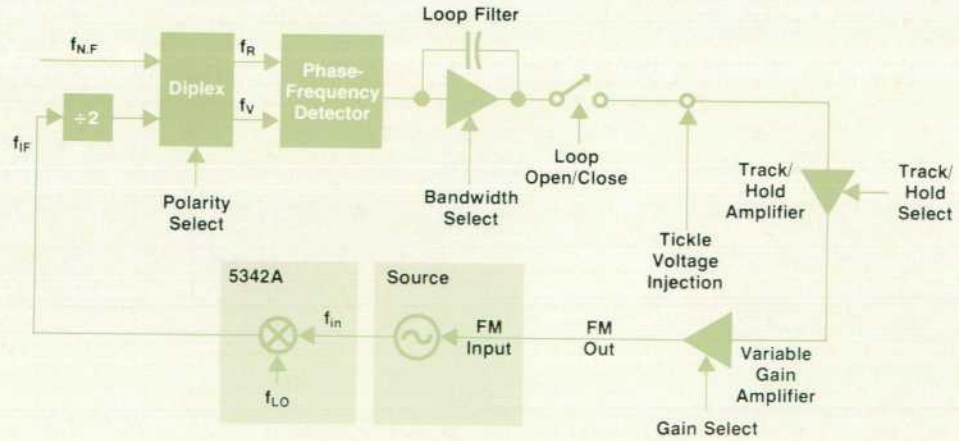

Fig. 4. *5344A main phase-locked loop block diagram. Shaded elements are outside the 5344A.*

frequency sweeping fractional-N synthesizer are transferred to the microwave source being locked.

Fractional-N Synthesizer

Fractional-N frequency synthesis is a powerful extension of the traditional divide-by-N technique of frequency synthesis shown in Fig. 3a. Here the voltage-controlled oscillator (VCO) frequency is divided by N before being locked to the 100-kHz reference. The VCO can be locked in steps of 100 kHz by changing N, which must be an integer.

Fig. 3b shows the additional elements necessary to achieve locking at fractional harmonics of the reference frequency. In the fractional-N synthesizer, pulses may be removed from the VCO output before being counted in the divide-by-N circuit. For example, if 10 pulses per second are deleted, the VCO frequency must rise by 10 Hz on the average to keep the loop in lock. Thus, if N were 500, the average output frequency would be 500×100 kHz + 10 Hz, or 50.00001 MHz. The effect is as if the VCO frequency had been divided by an N equal to 500.0001, composed of an integer part, 500, and a fractional part, 0.0001. While the average frequency may be correct, each pulse removal causes the phase detector to detect a 360-degree phase error and introduce a large transient into the loop. The result on the VCO output spectrum would be spurious sidebands spaced at multiples of 10 Hz from the accurately synthesized carrier frequency. This problem is prevented by adding a correction current (called phase interpolation) to the output of the phase detector to compensate exactly for these transients. The required waveform is a sawtooth with the vertical portion coincident with the cycle removal.

Both the cycle removal circuit and the phase interpolator are controlled by a custom NMOS integrated circuit which calculates the required phase offset each time the phase is measured, which is on each cycle of the reference, or every 10 microseconds. This analog phase correction current is generated by a five-digit digital-to-analog converter. With this technique the ultimate frequency resolution attainable is limited only by the number of digits carried in the calculating circuitry, fifteen in this case. The quality of the output spectrum, on the other hand, is determined largely by the resolution of the phase interpolator. The spurious signals in the VCO output are held to at least 70 dB below the carrier.

Phase-continuous frequency sweeps are made possible by adding a small frequency increment each time the phase offset is calculated. Since this occurs at a rate (100 kHz) that is high compared to the loop bandwidth (about 7 kHz), the resulting frequency steps are smoothed, that is, there are no phase transients during the sweep. Another register keeps track of any marker frequency entered and a TTL pulse signals the microprocessor as that frequency is passed. The microprocessor uses this pulse to generate a marker pulse on the 5344S Z-axis output.

Phase-Locked Loop

The phase-locked loop, which ultimately provides the synchronization of the source, is diagrammed in Fig. 4. Its purpose is to generate the FM correction voltage necessary to adjust the source output frequency so that its down-converted replica f_{IF} is in phase lock with the local synthesizer $f_{N,F}$.

The diplexer, which precedes the phase detector, allows the roles of the two phase-detector inputs to be reversed as necessary, according to the desired FM output polarity, that is, depending on whether a positive voltage makes the source tune up or down and whether the system is using the upper or the lower sideband for down-conversion.

The dynamic response of any feedback loop is highly dependent on the loop gain—the combined gain and phase shift of each component in the loop. Since the source to be synchronized is in the loop, we must know its FM tuning sensitivity and polarity and compensate for them. These parameters are measured before the loop is closed by impressing a small "tickle" voltage, −192 mV, on the source, measuring its output frequency, then removing the voltage and measuring again. The sensitivity is calculated from these measurements and the variable-gain amplifier in Fig. 4 (an 8-bit multiplying digital-to-analog converter) is adjusted to compensate. Thus, the loop gain is held

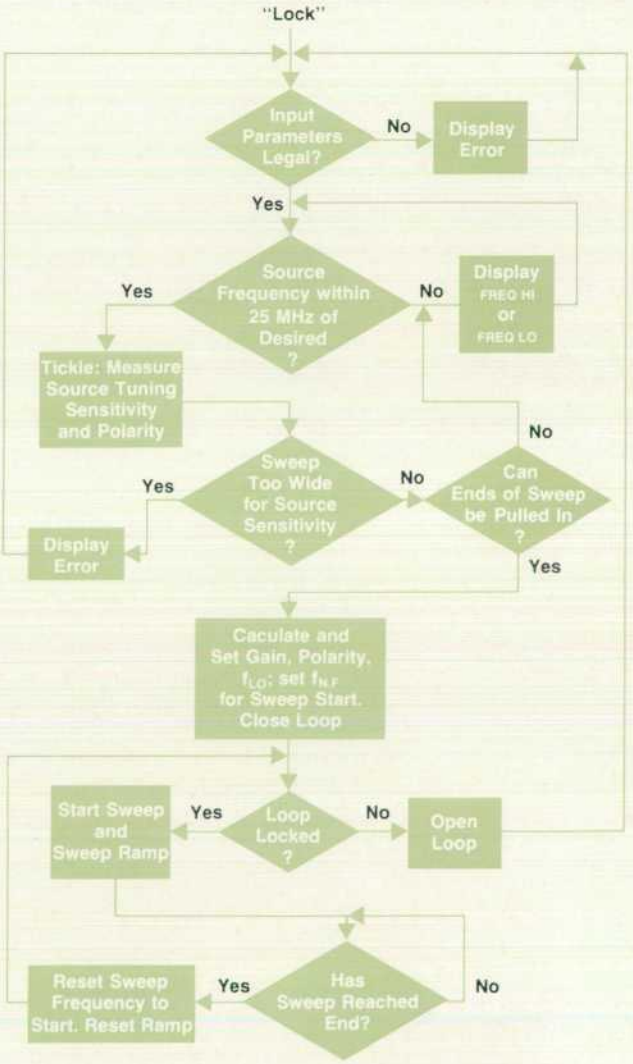

Fig. 5. *This lock algorithm is followed after the sweep parameters have been entered and the* ***MANUAL LOCK*** *button pressed.*

constant for any FM tuning sensitivity from 1 to 50 MHz per volt.

Lock Algorithm

Fig. 5 shows the algorithm used by the 5344S to prepare for and execute a repetitive phase-locked sweep after the start and stop frequencies and sweep time have been entered and the **MANUAL LOCK** button has been pressed.

First the input parameters are checked to be sure that the combination of start and stop or center and delta frequencies does not produce a disallowed result, such as an out-of-bounds frequency, a sweep that is too wide, or a backwards (high to low) sweep. Then the frequency of the source is measured and compared to the center of the desired sweep. If it is not within 25 MHz, a FREQ HI or FREQ LOW indication is given and the machine waits for it to be adjusted. If AUTO LOCK is used, the 5344S makes this coarse adjustment itself via the HP-IB. With the frequency now close to the desired value, the 5344S measures the source FM tuning sensitivity and polarity, and checks to see if the sweep is too wide for this sensitivity. Since the 5344S has ±10 volts of FM output available, sweep widths may be limited if source FM sensitivity is limited. Sweeps that cannot be accomplished with ±5 volts are disallowed. Thus, full sweeps of 40 MHz are possible only for source sensitivities of 4 MHz/volt or more. Furthermore, the synchronizer must ensure that the tuning voltage is adequate to achieve lock at each end of the sweep, which may mean that the unlocked source will need to be tuned closer than ±25 MHz. The possible pull-in or lock acquisition range is reduced by one-half the width of the sweep to 5 MHz worst-case. For example, if the user has requested a 40-MHz-wide sweep and the free-running source frequency is 5 MHz above the center of the sweep, the tuning voltage must pull the source down 25 MHz to reach the low end of the sweep. This is the limit of the pull-in range. For this example the source FM sensitivity must be at least 5 MHz/volt.

In case of any problem the 5344S tells the user that the source frequency is high or low or that the selected sweep parameters are impossible to achieve. With the source now coarsely tuned, the 5344S proceeds to set its internal synthesizers and loop gain and polarity, and then closes the loop. After waiting two milliseconds, the processor enables an out-of-lock interrupt. From this point on, any condition that unlocks the loop will interrupt the processor and restart the lock algorithm from the beginning.

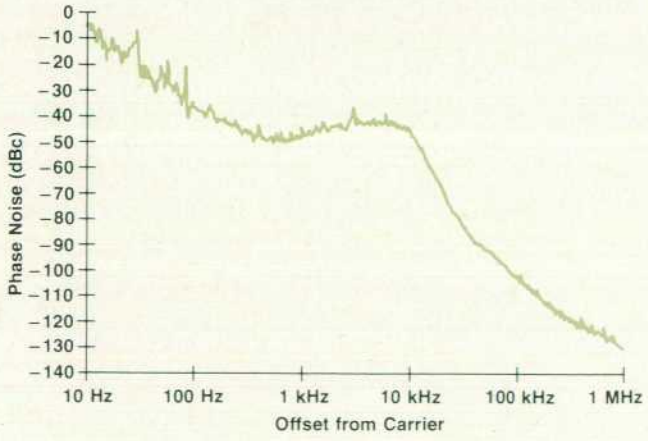

Fig. 6. *Single-sideband phase noise of an HP 8350A Sweep Oscillator with 83595A RF Plug-in, phase-locked by the 5344S at 5.76 GHz. (1-Hz bandwidth).*

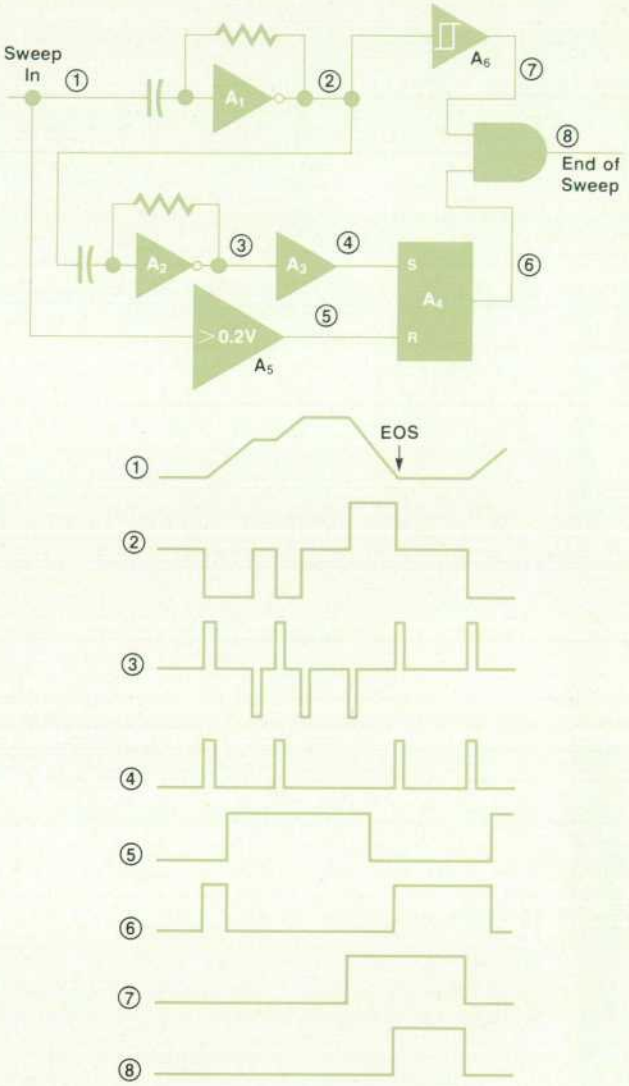

Fig. 7. *End-of-sweep detection in lock-and-roll mode.*

The fractional-N synthesizer, which was set for the start frequency of the sweep, is now triggered to start its sweep up. Simultaneously the sweep ramp is started. This is a 0-to-10-volt digitally generated ramp, synchronous with the sweep, sent to the **SWEEP OUT** port for display use. When the sweep ends, the frequency and ramp are simply reset to the beginning and restarted.

Phase Noise

The phase-noise characteristics of the synchronized source depend on both the unlocked source spectrum and the contributions of the 5344S. A phase-locked loop is effectively a low-pass filter to the noise of the reference signal (the 5344S), and a high-pass filter to the noise of the VCO (the source to be synchronized), with the same cutoff frequency in both cases. Thus, we would like a wide loop

bandwidth to lock a source that is much noisier than the 5344S, and conversely, a narrow bandwidth for relatively clean sources. The 5344S offers a choice of two bandwidths, 10 kHz and 100 kHz. Virtually all signal generators can use the 10 kHz position and most sweep oscillators, at least at the higher frequencies, need the 100 kHz loop bandwidth. Since the narrower loop has a very slow slew rate, however, it is not suitable for either phase-locked sweeps or lock-and-roll operation.

Fig. 6 shows the phase noise of an HP 8350A Sweep Oscillator with an 83595A plug-in phase-locked by the 5344S at 6 GHz.

Lock-and-Roll Operation

Lock-and-roll operation is really a simple extension of CW operation. This feature is largely realized by firmware with only two key pieces of extra hardware necessary. With an HP sweep oscillator such as an 8350A or 8620C set to a sweep mode with external triggering, and the 5344S set for the desired start frequency, the 5344S first triggers one sweep and waits for it to complete. This is to assure that the sweeper is waiting at the start of the sweep when the algorithm begins. The counter then checks to see that the frequency is within pull-in range, and if it is, the 5344S proceeds to lock just as in CW mode, that is, it checks tuning sensitivity and polarity, calculates frequencies and sets the internal synthesizers, closes the loop and checks to ensure that lock has been achieved. If it has, the track-and-hold circuit (Fig. 4) holds the correction voltage and the sweep is triggered. The instrument then simply waits until the sweep ends and the retrace has been detected (by a circuit to be described shortly). The frequency is now back at the start, so the FM correction voltage is released, the source locked, and the sweep repeated.

The FM correction voltage is held constant by the track-and-hold circuit throughout the sweep, although it may change from sweep to sweep. In other words, whatever correction was necessary at the start frequency is applied throughout the sweep. This makes sense for oscillators with very linear tuning-voltage-versus-frequency functions such as YIG-tuned oscillators. With this technique, the frequency error for broad sweeps can be reduced by as much as 80% to about 8 MHz for HP sweepers.

End-of-Sweep Detection

When the 5344S is in lock-and-roll mode, it knows when a sweep and retrace have been completed, and therefore when to relock the start frequency, by watching the sweeper's 10V ramp (SWEEP OUT) output signal, which looks like waveform 1 in Fig. 7. The ramp sweeps from approximately 0 volts to 10 volts as the frequency sweeps from start to stop, and contains pauses if the sweeper stops to change bands. A sweep may last from 10 milliseconds to 100 seconds. This signal is also output on the **SWEEP OUT** port of the 5344S in lock-and-roll mode for use as the horizontal drive for a display device such as an oscilloscope or X-Y plotter. It is replaced by an internally generated 10-volt ramp when the 5344S is in a phase-locked sweep mode.

The end-of-sweep point (marked EOS in waveform 1, Fig. 7) is extracted from the ramp by looking for the inflection point. To do this, the waveform is differentiated twice in A_1 and A_2. To accommodate the four-decade range in sweep rates, A_1 is piecewise linear, that is, its gain changes in three steps as the input voltage slope changes. Comparator A_3, set to zero volts, selects the positive portions of waveform 3 so its output contains a pulse at each positive inflection of the input waveform, and this serves to set the set-reset flip-flop A_4. Flip-flop A_4 is reset (resets override set inputs in this device) by comparator A_5 whenever the input waveform is above 200 millivolts, thus eliminating inflections that are not near ground potential. Comparator A_6 (with hysteresis) selects descending portions of the waveform and when gated with waveform 6 eliminates inflections that do not follow a negative slope. The result is waveform 8, which contains a positive transition at the positive inflection point of a negative slope near ground, the end of the sweeper's retrace.

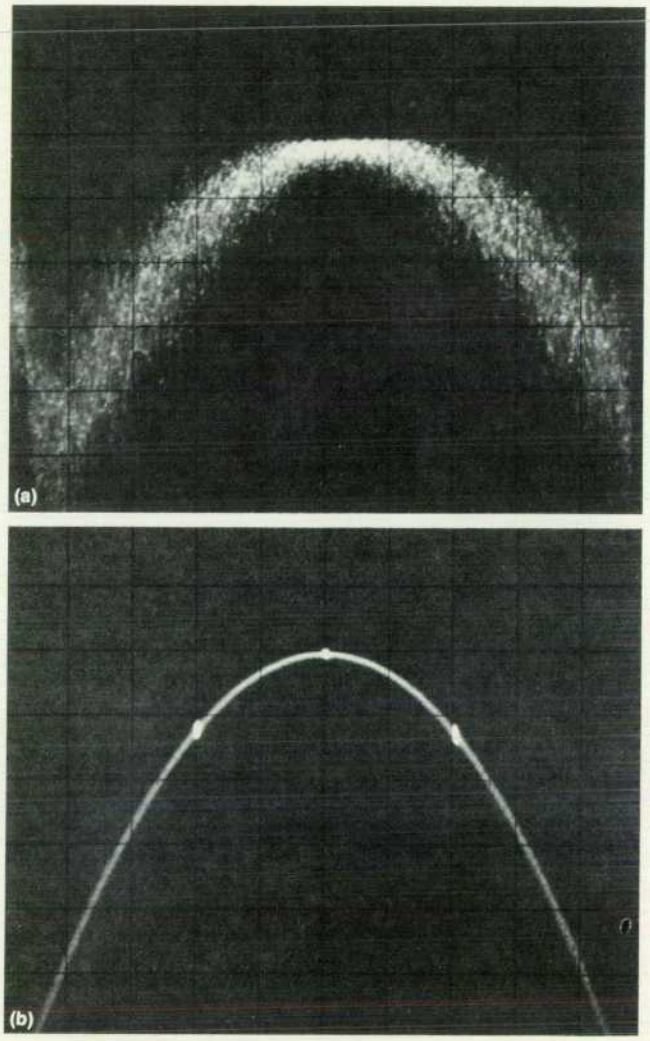

Fig. 8. *(a) Insertion loss of a high-Q surface-acoustic-wave resonator. Vertical scale: 0.25 dB/div. Horizontal scale: 100 kHz sweep width. The sweep oscillator's residual FM interferes with the measurement. (b) Same measurement with the sweeper locked by the 5344S Source synchronizer. Markers showing passband edges and center frequency are at 749.760000 MHz, 749.780000 MHz, and 749.800000 MHz.*

Testing Narrow Devices

The extraordinary accuracy of the phase-locked sweep mode with its four markers has proved very useful for testing or adjusting components with high accuracy requirements, such as narrow communications filters. Using the source synchronizer with a microwave source and a network analyzer, the source may be swept across a device's passband and markers placed on critical points with assurance of synthesizer accuracy. If the analyzer is automatic, such as the HP 8755P, the whole process may be automated via the HP-IB, which is standard on the 5344S.

Measurements on extremely narrowband devices are sometimes made difficult by the residual FM of the swept source being used. Fig. 8a shows the passband insertion loss of a high-Q surface acoustic wave resonator at approximately 750 MHz. The residual FM of the sweeper interferes with the examination of passband details. When the sweeper is locked with the 5344S (Fig. 8b) its residual FM is effectively eliminated and the markers allow precise determination of center or band-edge frequencies.

Acknowledgments

The author wishes to acknowledge the contributions of the capable people who worked on the 5344S. The idea was proposed and the project led in the early stages by Ali Bologlu. The analog circuitry was designed by Alan Tarbutton and the digital circuitry by Grady Hamlett. Jon Selden, Cathrin Callas and Lisa Stambaugh wrote the 16K bytes of firmware in the instrument. Keith Leslie did the product design. Marketing efforts were handled by Craig Artherholt, and production engineer Scott Gibson contributed much to the smooth introduction of the 5344S. The fractional-N synthesizer design was adapted from the HP 3325A, designed in the lab of the Loveland Instrument Division.

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Al Barber has been designing microwave counters and related products since he joined HP in 1968. He has contributed to the design of the 5341A, 5342A, and 5354A Counters and the 5344S Source Synchronizer, and served as project leader in the final phases of the 5344S project. Al was born in Chicago and grew up in Fairbanks, Alaska. He received his BSEE degree from the University of Washington in 1968 and his MSEE from Stanford University in 1970. He lives in San Jose, California and enjoys skiing, mountain climbing, and aerobatic flying.

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