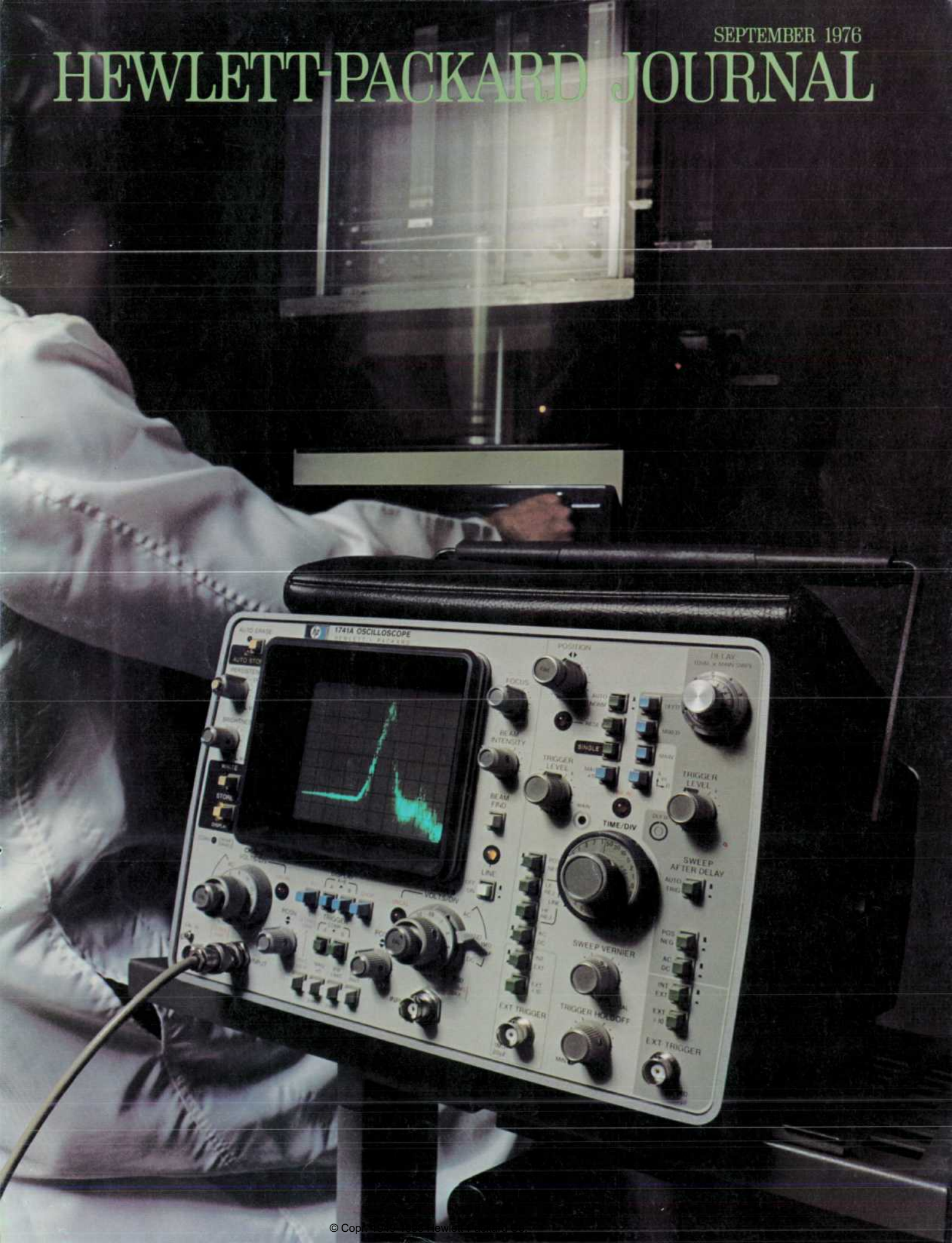


SEPTEMBER 1976

# HEWLETT-PACKARD JOURNAL





# An Easier-to-Use Variable-Persistence/Storage Oscilloscope with Brighter, Sharper Traces

*Revising the control arrangement and operating modes of a variable persistence oscilloscope results in a more "friendly" instrument that also has improved display characteristics.*

by Van Harrison

**V**ARIABLE PERSISTENCE-STORAGE oscilloscopes enable a user to view and measure occasional signal transients that escape detection with conventional oscilloscopes. Now with improved writing rates, variable persistence/storage scopes have become fast enough to permit their general use in the high-speed transient analysis that often accompanies digital design and troubleshooting, especially for finding "glitches" that occur randomly (Fig. 1).

The variable persistence/storage scope also retains waveforms traced at very slow sweep speeds, allowing the user to see the entire waveform rather than a moving dot (Fig. 2). With persistence adjusted to overlap traces, these instruments can integrate fast signals that occur at too low a repetition rate for normal viewing, making the signals brightly visible for examination (Fig. 3). In fact, this integrating technique makes it possible to view signal transitions that are much faster than the basic writing rate of the oscilloscope.

In view of all these advantages, in addition to the ability to do everything that conventional scopes can do, the question arises: why aren't variable persistence/storage scopes used more often? Part of the answer may be cost. They do cost more. But more than that may be the duller, fuzzier trace, the esoteric controls—these intimidate the casual user—and the tediousness of setting up the instrument for storage. Then too there has been the fear of burning the storage surface of an expensive-to-replace CRT.

A new variable persistence/storage scope (Fig. 4) has been designed to make this type of instrument more acceptable to the average user by eliminating most of these problems. A new arrangement of the controls with LED indicators to show what state the instrument is in takes some of the mystery out of instrument operation. Auto store and auto erase modes of operation simplify instrument use. Improvements in the CRT result in a brighter trace that is

more sharply focused, with trace quality as good as or better than that of some comparably-performing conventional oscilloscopes (Fig. 5). Protection circuits reduce the likelihood of burning the storage surface while simplifying beam intensity and focus adjustments.

Basically, the new oscilloscope, Model 1741A, is identical to and can be used like the Model 1740A, described in the HP Journal, December 1975, with the added advantages of variable persistence and storage. Both scopes are dual-channel, delaying sweep oscilloscopes with dc-to-100-MHz response, 5-mV/div



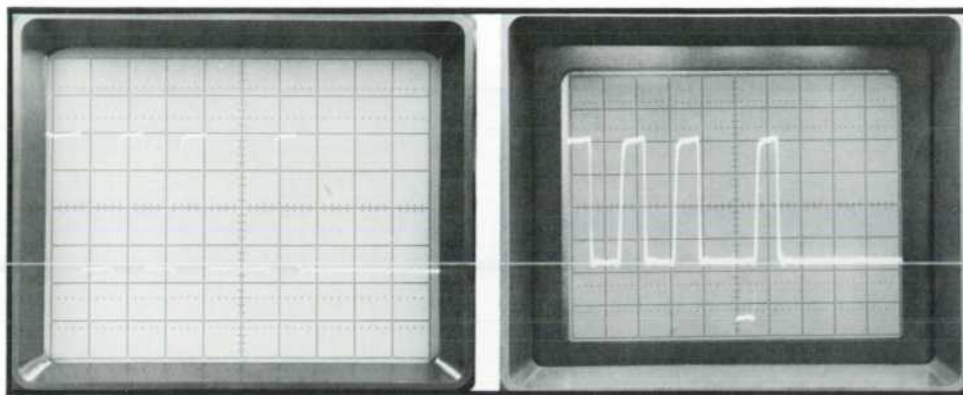
**Cover:** A shock-test machine slams down to test an instrument's ruggedness, an accelerometer responds to the resulting G forces, and a variable-persistence/storage oscilloscope captures the single accelerometer pulse so its magnitude can be measured. This is one of the applications for which this type of oscilloscope is uniquely suited. The HP Model 1741A variable-persistence/storage scope, shown here is described in the article beginning on this page.

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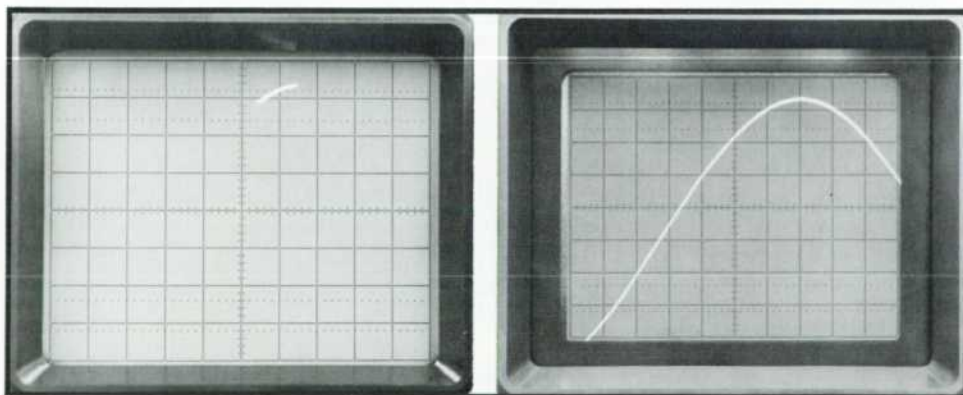
**Fig. 1.** By overlapping several successive traces, variable persistence oscilloscopes can disclose the existence of intermittent glitches that escape detection by other means. The glitch that occasionally follows the third pulse in this pulse train is not visible on a conventional oscilloscope display (left) but becomes visible on a variable persistence oscilloscope (right).

minimum deflection factor (1 mV/div with magnifier on), selectable input impedance (50 $\Omega$  or 1 M $\Omega$ /20 pF), and a third trace for viewing the triggering waveform. To these basic performance characteristics, the Model 1741A adds variable persistence and storage with a writing rate of >100 cm/ $\mu$ s in both variable persistence and storage modes of operation, fast enough to capture a single transient pulse less than 20 ns wide and taller than 1 graticule division.

these controls.

As shown by the timing diagram of Fig. 6, in the AUTO ERASE mode a sweep trigger unblanks the CRT beam and starts the horizontal sweep circuit, writing a trace. At the end of the sweep, the CRT beam is blanked and control is handed to the storage circuits, which inhibit further sweep triggering while displaying the stored trace.

The trace remains on view for a time ( $t_2$ ) between

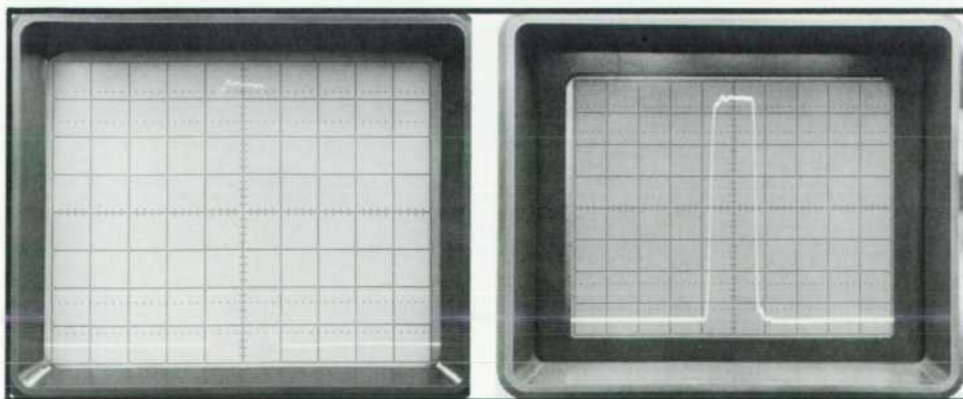


**Fig. 2.** Slow-moving waveform (10 ms/div) shows up as a moving dot on a conventional oscilloscope (left) but the waveform is easily seen on a variable-persistence/storage oscilloscope (right). CRT persistence can be adjusted so the waveform is retained just until a new trace is written.

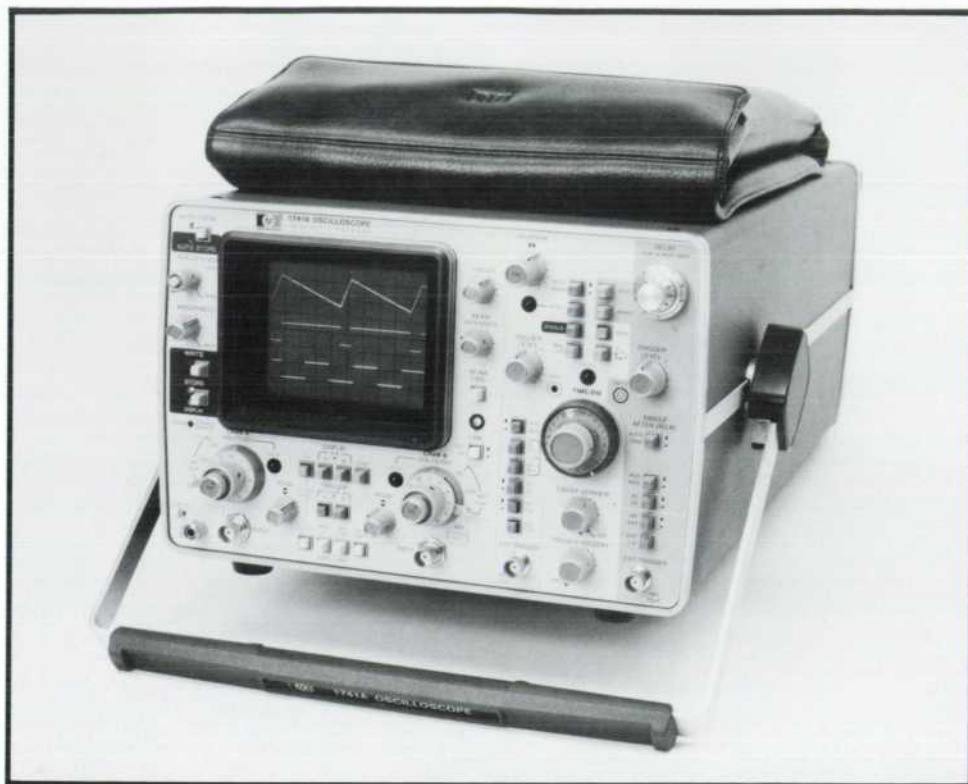
### Auto Erase

The new oscilloscope has an AUTO ERASE mode that, by automating the erase/write/view cycle, facilitates the setting of the CRT controls for optimum brightness and focus. This mode permits the operator to quickly evaluate the effect of any changes made to

1 and 10 seconds, selectable by the VIEW control. At the end of the view time, the instrument switches to the ERASE mode, wiping out the trace. After 300 ms, control is handed back to the sweep circuits which then await another trigger. The AUTO ERASE circuit allows two sweeps between erasures when the in-



**Fig. 3.** Fast waveform transitions occurring at a low repetition are barely visible on a conventional oscilloscope (left) but become brightly visible when several repetitions are integrated by a variable persistence oscilloscope (right). Sweep time here is 50 ns/div and the repetition rate is 50 sweeps/s.



**Fig. 4.** New Model 1741A Oscilloscope has variable persistence and storage modes of operation in addition to having all the other attributes of a high-quality, laboratory grade, 100-MHz Oscilloscope. Storage controls, with LED indicators to show what state the instrument is in, are grouped conveniently to the left of the CRT.

strument is in the alternate sweep mode, and three sweeps if the TRIGGER VIEW mode is added. Dual- or triple-channel displays are thus possible in the AUTO ERASE mode.

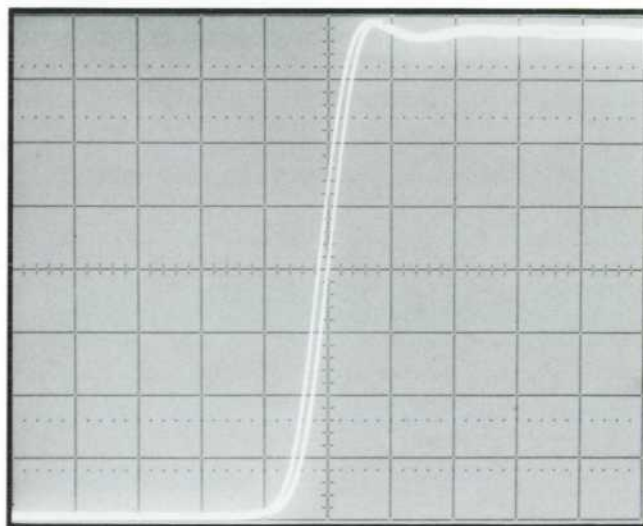
Besides permitting the operator to adjust the CRT beam controls quickly for optimum settings before making a transient measurement, the AUTO ERASE mode is also useful as a repetitive single-shot mode for examining the voltage levels and transition times of random binary sequences, for examining high-frequency signals contaminated with time jitter or low-frequency noise, or for examining the characteristics of other types of signals that are obscured in normal oscilloscope operation when successive traces are not identical (Fig. 7).

#### Auto Store

One limitation in the application of storage scopes has been the length of time that the CRT can wait in a state prepared to capture a transient when looking for powerline transients, power supply transients, or any other transients or noise that occur at unpredictable times. This wait time, usually about 30 seconds, was the time it took for the CRT screen to fade positive (become illuminated all over), washing out any trace that might subsequently be written.

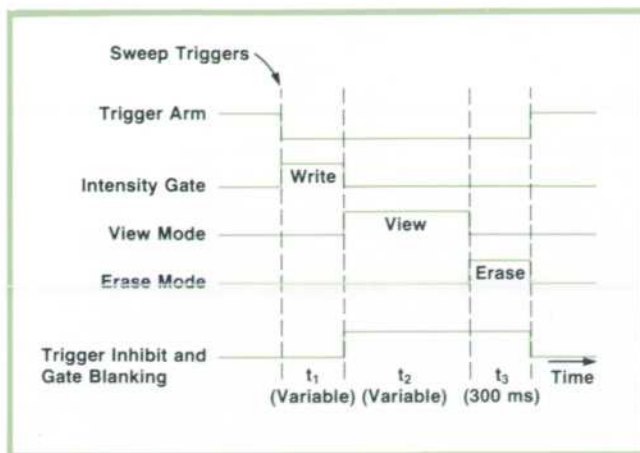
The AUTO STORE mode of the Model 1741A extends this wait time to several hours. As shown by the timing diagram of Fig. 8, the instrument remains in the ERASE mode (time  $t_1$ ) while the sweep trigger

circuit waits in the armed state. As soon as a trigger occurs, the instrument switches automatically to the WRITE mode and the sweep starts. When the sweep terminates, the instrument switches to the STORE mode and retains the written trace up to 30 minutes for examination. Front-panel LED indicators show what state the instrument is in, clearly indicating when the scope is triggered and when it switches to



**Fig. 5.** Exceptionally fine traces are obtained on the Model 1741A in variable persistence and storage modes of operation. The two waveforms traced here while the instrument was in the variable persistence mode are separated horizontally by only 1.7 mm (sweep time is 5 ns/div).





**Fig. 6.** In AUTO ERASE mode, trace writing, viewing, and erase occur repetitively.

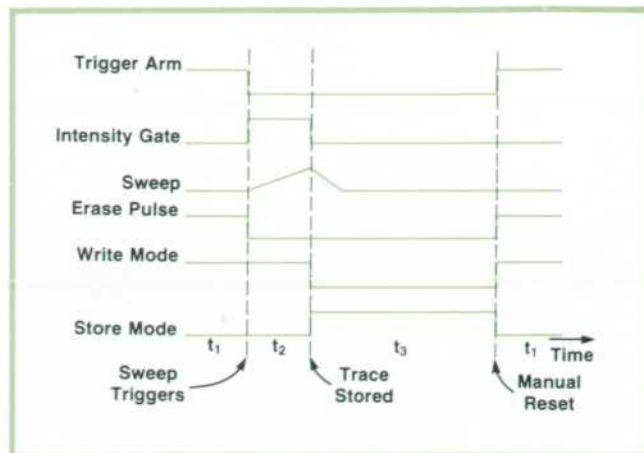
STORE. Pressing the STORE/DISPLAY button makes the trace visible for viewing. Storage time in the DISPLAY mode, however, is reduced to 10 to 30 seconds depending on the setting of the BRIGHTNESS control.

To keep front-panel clutter at a minimum, the AUTO ERASE and AUTO STORE modes are selected by the same pushbutton, LED indicators showing which mode is selected (see Fig. 4). Depressing this button selects the AUTO STORE mode if the SINGLE SWEEP pushbutton is also pressed. Otherwise, the AUTO ERASE mode is selected. Releasing the button returns the scope to normal variable persistence operation.

#### Intensity Limit

The storage surface of storage CRTs can be damaged by excessive beam current. The possibility of this happening is reduced in the Model 1741A even though the beam current can be set high enough to achieve a  $100 \text{ cm}/\mu\text{s}$  single-shot writing rate. An intensity-limit circuit monitors the CRT beam current and limits the average current to a safe level.

A diagram of the intensity-limit circuit is shown in Fig. 9. Resistor R1 is in series with the cathode-ray gun accelerator anode. When the anode current, which is approximately proportional to total beam



**Fig. 8.** In AUTO STORE mode, oscilloscope waits in the ERASE mode until the sweep triggers. At the conclusion of the sweep, the instrument switches to the STORE mode to retain the trace.

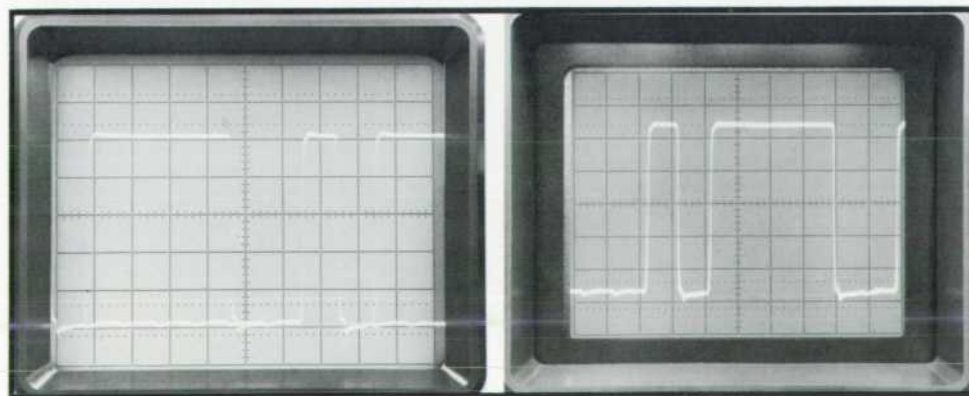
current, is sufficient to cause the voltage drop across R1 to turn on transistor Q1, Q2 restrains the voltage at the wiper of the INTENSITY control from going any further negative, keeping the CRT beam current at or below this level.

Capacitors C1 and C2 average the voltage across R1 so the very low average of fast single-shot or low-duty cycle signals does not restrict the beam current, permitting maximum writing rate and bright display of these signals. The averaging also provides an automatic intensity correction when changing sweep speeds as, for example, when switching from main sweep to a much faster delayed sweep.

#### Auto Focus

Normally, a change in CRT beam current requires a readjustment of the FOCUS control. AUTO FOCUS allows the intensity-limit system to alter the beam current without requiring any adjustment of the FOCUS control.

The change in focus voltage required by a change in beam current is diagrammed in Fig. 10. This curve is approximated by the circuit of Fig. 11. A voltage



**Fig. 7.** Signals that do not repeat identically are difficult to analyze on a conventional scope (left), but can be presented in a repetitive single-shot mode (right) when the Model 1741A is operating in the AUTO ERASE mode.



## A Brighter, More Sharply Focused Variable Persistence/Storage Cathode-Ray Tube

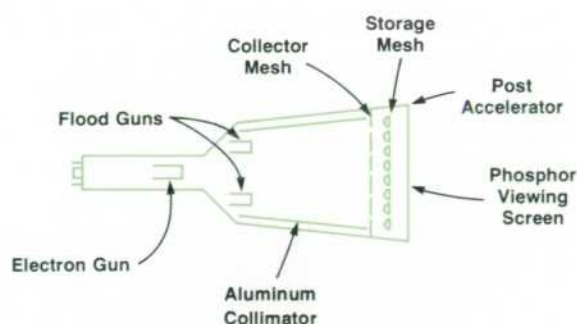
Variable persistence/storage CRTs, originally developed for radar applications, retain oscilloscope traces on a storage mesh located precisely 0.08 inch behind the phosphor surface. The mesh is a fine metallic screen coated with a dielectric (magnesium fluoride).

When a trace is to be stored, the storage surface is brought to  $-10$  V. Electrons in the CRT beam strike the surface with sufficient energy to dislodge several electrons for each electron in the beam, raising the potential of the storage surface where the beam strikes. The dislodged electrons are swept up by the positively charged collector mesh nearby (see drawing).

CRT beam electrons that pass through the storage mesh strike the phosphor surface, generating a trace that shows where writing occurs. After completion of the sweep, the stored trace is made visible by flood-gun electrons. The low-velocity electrons from the flood guns are repelled by negatively charged areas of the storage surface and gathered by the collector mesh, but where the storage surface has been charged by the electron beam, the electrons approach close enough to the mesh to be pulled through by the high accelerating potential of the phosphor surface ( $5.2$  kV), striking the phosphor with sufficient energy to produce a visible trace.

To erase the stored trace, the storage mesh is raised to the same potential as the collector electrode ( $+156$  V) for  $50$  ms. The entire storage surface then becomes uniformly charged, obliterating the trace. The storage surface is then returned to  $-10$  V for the next write cycle.

Variable persistence is obtained by shortening the erase cycle so only partial erasure occurs. The erase cycle repeats at a  $1$ -kHz rate so the trace slowly fades from view. By varying the width of the erase cycles, the rate of fade can be controlled



within a range of  $100$  ms to  $1$  minute.

During the view phase, the few inevitable gas molecules in the CRT become ionized. These collect on the storage mesh, slowly bringing the non-written areas of the storage mesh up to the potential of the written area, washing out the trace. This limits storage time in the view mode to about  $30$  seconds. Increasing the viewed brightness accelerates this process so there is a trade-off between trace brightness and storage time in the DISPLAY mode.

### Taking a CRT One Step Further

The design of the CRT for the Model 1741A Oscilloscope is based on this same scheme, the CRT used in the Model 184A

Oscilloscope being taken as a starting point for the design. The major design goal for the new tube was to increase full-area writing rate. Within limits, writing rate can be improved by increasing the accelerating potential in the electron gun. The consequent increase in the electron beam energy results in a higher secondary emission ratio of the storage surface, and hence in a faster writing rate.

To meet design goals within a reasonable development time, it was decided to retain the successful manufacturing techniques developed for the storage elements in the Model 184A CRT and concentrate design efforts on obtaining higher electron beam energy from the electron gun. Unfortunately, deflection sensitivity is adversely affected by higher beam energy so the major effort was concerned with optimizing this trade-off.

To begin with, some loss in deflection sensitivity could be tolerated because the Model 1741A's deflection amplifiers are capable of higher drive voltages than those of the Model 184A. Nevertheless, the tube length was increased by  $34$  mm with the extra length being applied to the deflection-plate-to-phosphor-surface distance to increase deflection sensitivity.

With the new tube dimensions, the flood guns are further from the screen, improving flood-gun display uniformity. To further improve uniformity, the flood gun grid leads were brought out separately on neck pins to enable balancing of the flood gun outputs.

The deflection plates themselves were redesigned using calculator programs that clearly showed the various trade-offs between operating voltages, deflection plate dimensions, frequency response, and the other parameters that affect performance. From this a deflection plate shape was derived that allowed the closest possible spacing for maximum sensitivity without intercepting the beam.

The electron gun was reportioned to realize greater beam current while optimizing spot size, using curves published by Hilary Moss.<sup>1</sup> This resulted in a shorter anode that intercepts fewer electrons, leaving more beam current. The shortened anode also permitted a further increase in the deflection-plate-to-phosphor spacing.

All of these steps increased deflection sensitivity to the point that the cathode potential could be increased  $855$  volts to  $-2295$  V. The result was a substantial increase in beam current and, consequently, in writing rate ( $>100$  cm/ $\mu$ s). Cut-off voltage is  $-100$  V, allowing a large drive voltage with high beam current in the single-shot mode (the intensity-limit circuit holds the drive to lower levels in repetitive operation).

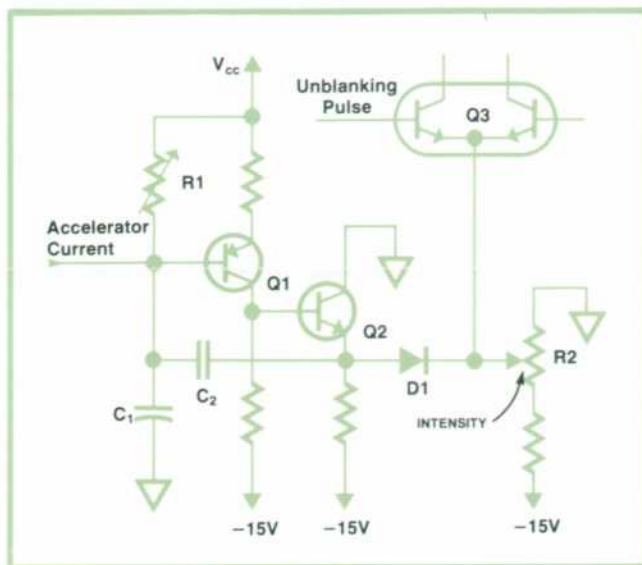
### Acknowledgments

Many people contributed to the design of the new CRT. Johan Sverdup and Chuck Gustafson provided continuing encouragement and guidance. Special thanks are due Roy Wheeler, Dave Granteer, and Jim Haley for valuable technical advice and programming assistance. Much help was also provided by John Hawton, Paul Carnahan, Frank Balint, and Hank Ragsdale.

-Robert G. Wickliff Jr.

### Reference

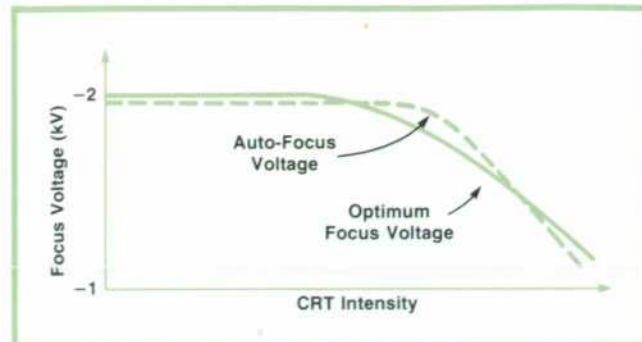
1. H. Moss, "Narrow Angle Electron Guns," Academic Press, New York and London, 1968.



**Fig. 9.** Intensity-limit circuit responds to the average current in the electron-gun anode and limits the excursions of the CRT unblanking pulse accordingly.

proportional to intensity is taken from the INTENSITY control (R2 of Fig. 9) and buffered by Q4 (Fig. 11). The turn-on threshold of transistor Q5 is set by potentiometer R6, and this threshold becomes the break point for the curve of Fig. 10. Above the break point the slope of the focus-voltage-vs-intensity-setting curve is determined by the ratio of R7 to  $R4 + R5$ . The focus-voltage-vs-intensity-setting curve is thus approximated closely enough that manual adjustment gains only marginal improvement, if any at all.

Model 1741A has a BRIGHTNESS control in addition to the INTENSITY control. The INTENSITY control adjusts CRT beam current whereas the BRIGHTNESS control, by determining the steady-state voltage of the

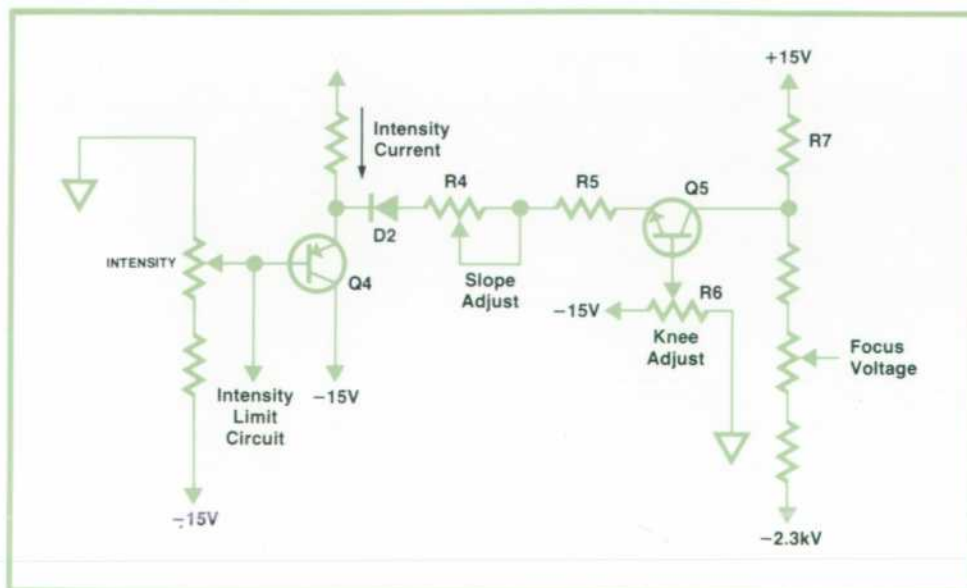


**Fig. 10.** Graph of the optimum focus voltage as a function of CRT intensity (solid line). The dotted line is the curve generated by the auto focus circuit (Fig. 11).

storage mesh, affects display intensity when viewing a stored trace. With the BRIGHTNESS control at its most negative position, the storage surface repels most flood-gun electrons, allowing only a few to be attracted by the phosphor voltage through the mesh where the trace is written. At its most positive level, many electrons pass through where the trace is written, giving a bright trace, but the display also fades positive more quickly. The BRIGHTNESS control permits the operator to find the best balance between trace brightness and viewing time. It replaces the MAX WRITE switch of earlier HP variable\_persistence/storage scopes which gave only two levels of control for this function.

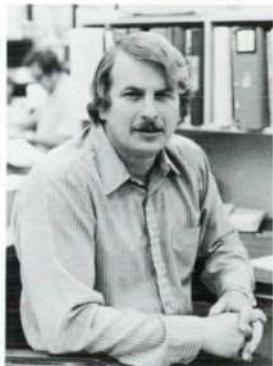
### Added Conveniences

Other features contribute to ease of operation. For instance, when the instrument is in the SINGLE SWEEP mode, pushing the manual ERASE button not only erases the trace but it also resets the sweep, eliminating the bother of pushing two different buttons to reset the instrument for a single-shot measurement.



**Fig. 11.** The auto focus circuit modifies the voltage applied to the focus control in response to the INTENSITY control setting.





### Van Harrison

Van Harrison spent two years with the U.S. Navy in Ethiopia before attending the University of Florida, where he obtained BSEE and MSEE degrees. Upon graduation (1972) he joined HP, contributing to the Model 1740A 100-MHz Oscilloscope before assuming project leadership of the Model 1741A. A native of Ormond Beach, Florida, Van is married and has two children. He also designs hi-fi equipment, does some wood-working, skis, and golfs.

Switching to either the AUTO ERASE or AUTO STORE mode automatically sets the instrument for maximum persistence. Switching to the AUTO ERASE mode also switches the trigger mode to NORM so the trigger circuit is not left in the AUTO mode, which could trigger the scope randomly.

A hold-off circuit is wired into the STORE function so that when the STORE button is pressed during a sweep, the instrument does not go into the STORE mode until the current sweep completes. This arrangement is particularly desirable for slow sweeps when operating in the AUTO ERASE mode as it permits the operator to push the STORE button whenever he

sees something he wishes to retain without losing part of the complete sweep.

### Conventional Operation

The manner of operating the CRT has been changed for conventional non-storage display. Formerly, during normal oscilloscope operation the voltage on the storage mesh was made negative ( $-30$  V) to repel flood gun electrons and prevent them from illuminating anything written on the storage surface. This also happened to reduce the intensity of the electron beam. In the new oscilloscope, the flood gun grids turn off the electron flow in the conventional mode. At the same time, the storage mesh is raised to the potential of the collector mesh ( $+156$  V) so no secondary emission occurs and traces are not stored.

### Acknowledgments

I would like to thank Stan Lang and Johan Sverdup for constant support, encouragement and many useful ideas during the project, Al Best for his leadership and support during the latter stages of the project, Joe Millard and Eldon Cornish for flexible vertical and horizontal designs that allowed for new control ideas, Jim Carner for the mechanical design, Dick Stone and Herman Hinton for their customer-oriented inputs, and Chuck Gustafson for his many hours of help in understanding the subtleties of storage CRTs.

## ABRIDGED SPECIFICATIONS HP Model 1741A Oscilloscope

### Vertical Display Modes

Channel A, channel B, channels A and B displayed alternately on successive sweeps (ALT) or by switching between channels at 250 kHz rate with blanking during switching (CHOP); channel A plus channel B (algebraic addition), and trigger view.

### Vertical Amplifiers (2)

Bandwidth and Rise Time at all deflection factors from 0°C to +55°C:

BANDWIDTH: (3 dB down from 6 div reference signal):

DC-COUPLED: dc to 100 MHz in both 50Ω and 1 MΩ input modes.

AC-COUPLED: approx 10 Hz to 100 MHz, 1 Hz with 10:1 divider probes.

RISE TIME:  $\leq 3.5$  ns, measured from 10% to 90% points of a 6 div input step.

### DEFLECTION FACTOR

RANGES: 5 mV/div to 20 V/div in 1, 2, 5 sequence.

VERNIER: continuously variable between all ranges, extends maximum deflection factor to at least 50 V/div.

POLARITY: channel B may be inverted, front panel pushbutton.

### INPUT RC (selectable)

AC OR DC: 1 MΩ  $\pm 2\%$  shunted by approx 20 pF.

50 OHM: 50Ω  $\pm 3\%$ .

### A + B OPERATION

AMPLIFIER bandwidth and deflection factors are unchanged; channel B may

be inverted for A - B operation.

DIFFERENTIAL (A - B) COMMON MODE: CMRR is at least 20 dB from dc to

20 MHz. Common mode signal amplitude equivalent to 8 divisions with one

vernier adjusted for optimum rejection.

### VERTICAL MAGNIFICATION (X5)

BANDWIDTH: (3 dB down from 8 div reference signal):

DC-COUPLED: dc to approx 30 MHz.

AC-COUPLED: approx 10 Hz to 30 MHz.

RISE TIME:  $\leq 12$  ns (measured from 10% to 90% points of 8 div input step).

DEFLECTION FACTOR: increases sensitivity of 5 and 10 mV/div settings by

factor of 5 for maximum sensitivity of 1 mV/div on channels A and B.

TRIGGER SOURCE: Selectable from channel A, channel B, composite, or

line frequency.

TRIGGER VIEW: Displays internal or external trigger signal. In Alternate or Chop

mode channel A, channel B, and trigger signals are displayed. In channel A or

B mode, Trigger View overrides that channel. Internal trigger signal amplitude

approximates vertical signal amplitude. External trigger signal deflection factor

is approx 10 mV/div or 1 V/div in EXT - 10. Triggering point is approx center

screen.

### Horizontal Display Modes

Main, main intensified, mixed, delayed, mag X10, and A vs B.

### TIME BASE RANGES

MAIN: 50 ns/div to 2 s/div (24 ranges) in 1, 2, 5 sequence.

DELAYED: 50 ns/div to 20 ms/div (18 ranges) in 1, 2, 5 sequence.

MAIN SWEEP VERNIER: continuously variable between all ranges, extends

slowest sweep to at least 5 s/div.

MAGNIFIER (X10): expands all sweeps by a factor of 10, extends fastest sweep

to 5 ns/div.

### TIME BASE ACCURACY

Sweep Time/Div

X1 10

50 ns to 20 ms

$\pm 3\%$   $\pm 4\%$

$\pm 2\%$   $\pm 3\%$

$\pm 3\%$   $\pm 4\%$

\*Add 1% for 50 ms to 2 s ranges.

\*Accuracy

X1 10

50 ns to 20 ms

$\pm 3\%$   $\pm 4\%$

$\pm 2\%$   $\pm 3\%$

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X1 10

50 ns to 20 ms

$\pm 3\%$   $\pm 4\%$

$\pm 2\%$   $\pm 3\%$

$\pm 3\%$   $\pm 4\%$

\*Add 1% for 50 ms to 2 s ranges.

\*Accuracy

X1 10

50 ns to 20 ms

$\pm 3\%$   $\pm 4\%$

$\pm 2\%$   $\pm 3\%$

$\pm 3\%$   $\pm 4\%$

\*Add 1% for 50 ms to 2 s ranges.



# An Automatic Wide-Range Digital LCR Meter

*Easy operation, a wide measurement range, two measurement frequencies, high reliability, optional HP-IB compatibility, and low cost make it suitable for a wide range of component and impedance measurements.*

by Satoru Hashimoto and Toshio Tamamura

**A** NEW DIGITAL LCR meter, Model 4261A (Fig. 1), is designed to provide the wide range and accuracy of a universal impedance bridge without the bridge's disadvantages of manual balancing and meter-reading ambiguity. The new LCR meter is fully automatic, displaying the value and dissipation factor of an unknown inductor or capacitor or the value of an unknown resistor on its 3½-digit display a fraction of a second after the unknown is connected to its terminals. Selection of the measurement equivalent circuit is made automatically according to the value of the unknown component.

The new LCR meter typically can take four or more readings per second at a 1-kHz measurement frequency and one or more at 120 Hz with basic accuracies of 0.2% for capacitance, inductance, resistance,

and dissipation factor. The unknown terminals are configured in a five-terminal arrangement that is capable of four, three, and two-terminal connections suitable, respectively, for low-impedance, high-impedance, and ordinary measurements. The unit measures capacitance from 0.1 pF to 1900  $\mu$ F at 1 kHz and from 1 pF to 19.00 mF at 120 Hz, inductance from 0.1  $\mu$ H to 190.0 H at 1 kHz and from 1  $\mu$ H to 1900 H at 120 Hz, resistance from 1 m $\Omega$  to 19.00 M $\Omega$  at 1 kHz or 120 Hz, and dissipation factor of capacitors or inductors from 0.001 to 1.900. For measurements in semiconductor, two test voltages, 50 mV and 1V rms, are available for making capacitance measurements in the parallel equivalent circuit mode. An internal dc bias source provides switch-selectable 1.5V, 2.2V, and 6V. External bias from 0V to 30V can be supplied



**Fig. 1.** Model 4261A LCR Meter makes fully automatic measurements of inductance, capacitance, resistance, and dissipation factor at 120 Hz or 1 kHz. It provides a choice of two test signal levels, three internal dc bias voltages, and two, three, or four-terminal measurement connections. HP Interface Bus (IEEE 488-1975) compatibility is optional.



to a rear-panel connector. An offset adjustment for canceling stray capacitance between the unknown terminals is provided; a capacitance offset signal, available at a rear-panel BNC connector, provides an offset range of 0 to 100 pF when fed into the low-current terminal through a variable capacitor.

A low-power design keeps total power consumption below 25 watts, helping to assure reliability. For automated testing or data gathering under computer or calculator control, an option provides an interface to the HP-IB (HP Interface Bus), HP's implementation of IEEE Standard 488-1975.

### How It Works

The 4261A measures L, C, R, and dissipation factor by determining the impedance or admittance of the unknown device under test (DUT). In the current-to-voltage converter section (Fig. 2), the measuring signal is applied to the DUT and an operational amplifier is used as a current detection amplifier. The current through the DUT is almost equal to that flowing in the range resistor  $R_R$ . Voltages  $e_1$  and  $e_2$  are obtained by detecting the voltages produced across the DUT and range resistor  $R_R$ , respectively, using differential amplifiers  $A_2$  and  $A_3$ .  $e_1$  and  $e_2$  are transferred to the measurement section, where their vector ratio is detected by a phase detector and a dual-slope analog-to-digital converter.

When a device is measured with the 4261A, either a series equivalent circuit mode or a parallel equivalent circuit mode is automatically selected. When the DUT impedance is relatively low the series mode is selected and when it is relatively high the parallel

mode is selected. In the series mode, the 4261A selects a source resistance at least ten times the value of the DUT impedance to achieve a constant current drive. When the parallel equivalent circuit mode is chosen, a source resistance less than one-tenth that of the DUT impedance is selected to drive the DUT at a constant voltage. The source resistor ( $R_0$ ) helps to limit current flow into the current detecting amplifier when its terminals are shorted, and to suppress differential or integral noise when a capacitor or inductor is connected.

For a  $C_p$ -D measurement in the parallel equivalent circuit mode,

$$e_1 = - \frac{(G_p + j\omega C_p)R_R}{1 + (G_p + j\omega C_p)R_0} e_0$$

$$e_2 = \frac{1}{1 + (G_p + j\omega C_p)R_0} e_0$$

where  $\omega = 2\pi f$ , and  $f$  = test frequency.

When  $e_2$  is the reference signal, the ratio of  $e_1$  and  $e_2$  is:

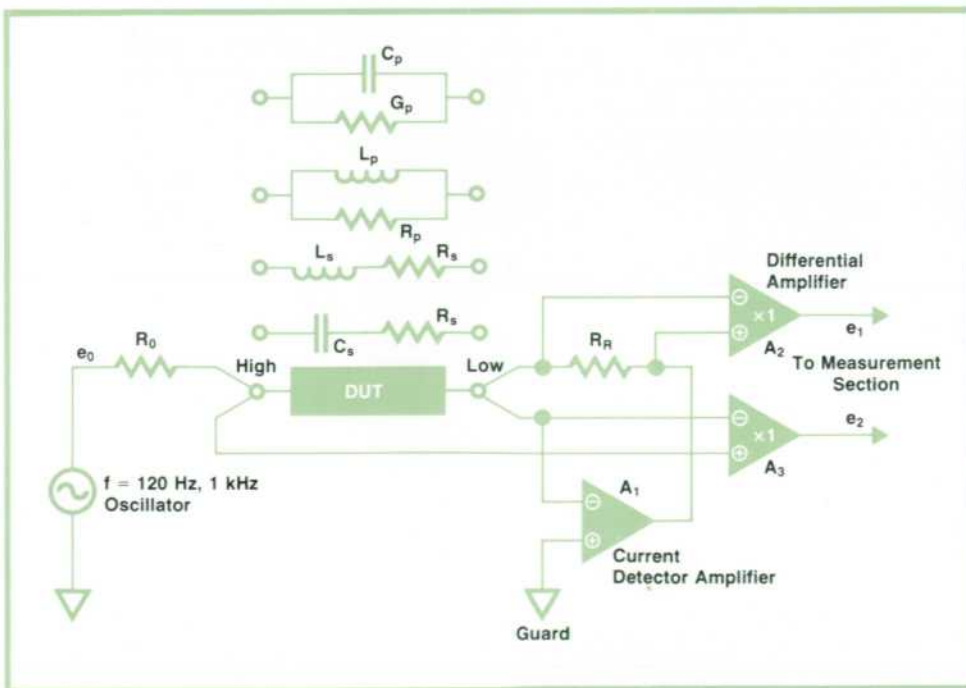
$$e_1/e_2 = - (G_p + j\omega C_p) R_R$$

which is proportional to the unknown admittance.

$L_p$ -D is determined in the same manner:

$$e_1/e_2 = - (1/R_p + 1/j\omega L_p) R_R$$

For a measurement in the  $L_s$ -D series circuit mode, the equations for  $e_1$  and  $e_2$  are:



**Fig. 2.** Current-to-voltage converter section applies the test signal to the unknown and develops two voltages,  $e_1$  and  $e_2$ , whose ratio is proportional to the unknown impedance or admittance. Selection of series or parallel equivalent circuit for the unknown is made automatically.



$$e_1 = - \frac{R_R}{R_0 + R_s + j\omega L_s} e_0$$

$$e_2 = \frac{R_s + j\omega L_s}{R_0 + R_s + j\omega L_s} e_0$$

When  $e_1$  is the reference signal, the ratio of  $e_2/e_1$  is

$$e_2/e_1 = - (R_s + j\omega L_s)/R_R$$

The equation for a  $C_s$ -D measurement becomes

$$e_2/e_1 = - (R_s + 1/j\omega C_s)/R_R$$

In all cases, the vector ratio multiplied or divided by  $R_R$  produces the DUT impedance or admittance. The 4261A has five range resistors (from 10  $\Omega$  to 100 k $\Omega$ ) having tolerances of 0.05%. It is possible to ignore the residual resistance of the range switch, which adds to  $R_R$  and might contribute to the error, since the current and potential terminals of the range resistors are separated. Detecting the voltage differentially minimizes the error contributed by the residual resistance of the lead connections to the DUT, and similarly, the residual voltage of the current detecting amplifier.

### Measurement Section

This section consists of a four-phase generator for phase detection, a sectional average integrator (SAI) that smooths the signal from the phase detector, a dual-slope analog-to-digital converter, and logic circuitry. The output is a digital quantity proportional to

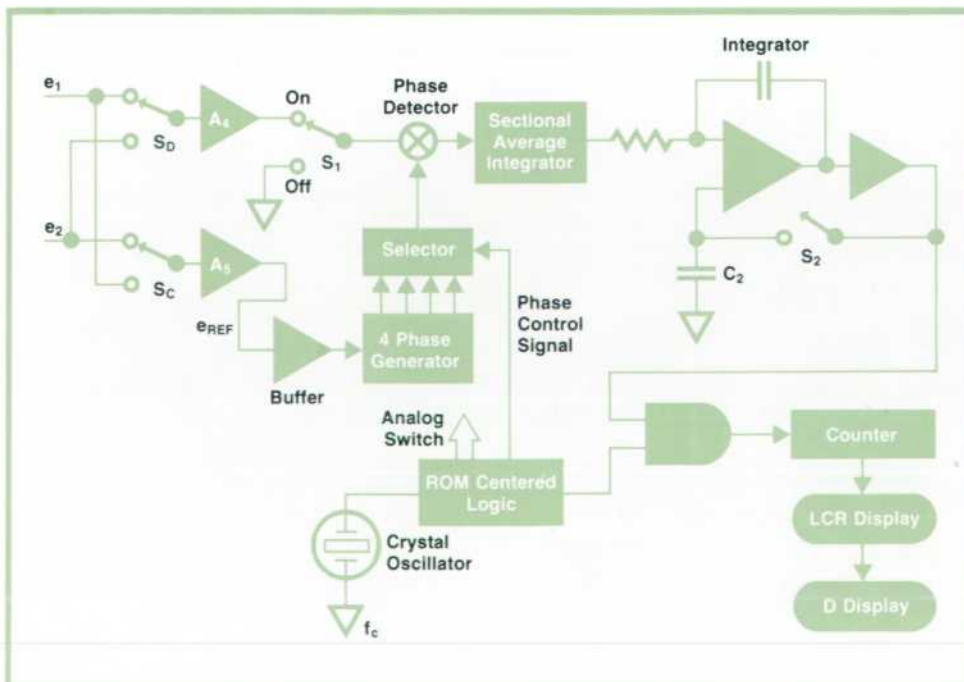
the vector ratio of  $e_1$  and  $e_2$ . A block diagram and timing chart for this section are shown in Figs. 3 and 4.

The instrument goes through a seven-step sequence to take a measurement. In step 1, an autozero is performed.  $S_1$  connects the input of the phase detector to ground and  $S_2$  is closed. Thus with no input ( $S_1$  is shorting the input to ground), the integrator loop is adjusted for zero input and the adjustment voltage is stored on  $C_2$ . This cancels any phase detector leakage current error as well as compensating for any dc offset voltage throughout the loop. During step 2, an auto phase adjustment is performed; this will be described later. Steps 1 and 2 are performed just before ratio detection.

Assume that a capacitor is being measured in the parallel circuit mode ( $C_p$ ).  $e_2$  is the reference signal, as previously described, and is applied to the four-phase generator. Step 3 is the integrator charging period  $T_1$ .  $S_1$  is on, and switch  $S_D$  is connected to  $e_1$ .  $e_1$  is then phase detected by a signal whose phase is shifted 90° from  $e_2$ , as determined by control logic in the ROM. The integrator charge ( $Q_{cp}$ ) stored during  $T_1$  is:

$$Q_{cp1} = -K\omega C_p R_R T_1 e_2.$$

where  $K$  is the product of the efficiency of the phase detector and the integrating constant. Step 4 is the integrator discharge cycle.  $S_D$  is connected to  $e_2$ , which is phase detected by a signal in phase with  $e_2$ . The integrator begins to discharge and continues discharging until its output crosses the zero-volt point. If the discharge time is  $T_{cp}$ , the charge dissipated is:



**Fig. 3.** Measurement section develops and displays a digital representation of the vector ratio of  $e_1$  and  $e_2$ .



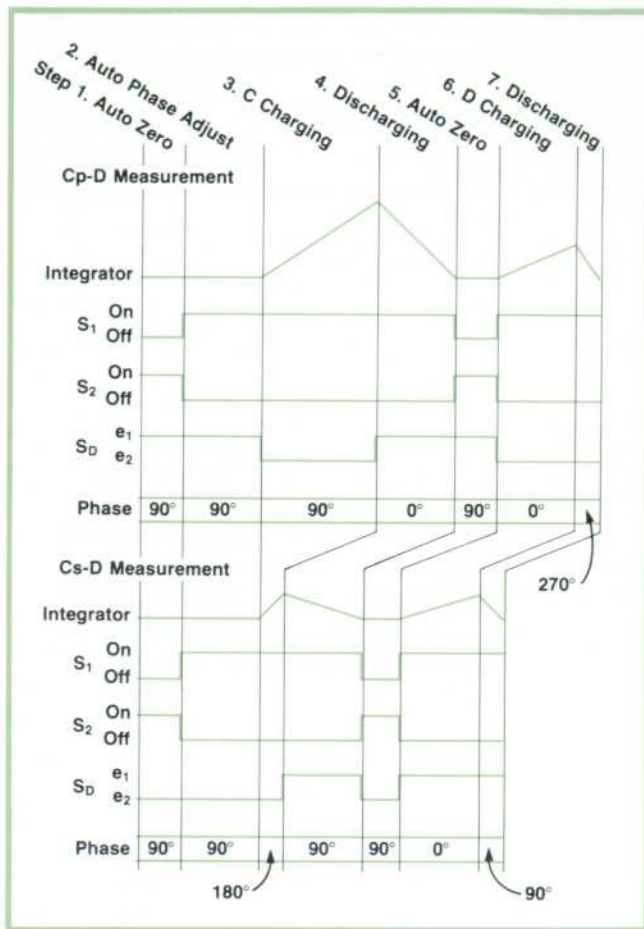


Fig. 4. The measurement sequence consists of seven steps including autozero and auto-phase-adjust steps. The dual-slope analog-to-digital conversion method is used, except that in the  $C_s$ -D measurement the slopes occur in reverse order.

$$Q_{cp2} = K T_{cp} e_2.$$

From steps 3 and 4,

$$Q_{cp1} = -Q_{cp2}$$

$$T_{cp} = \omega C_p R_R T_1.$$

$T_1$  is  $n_1$  times the period of the test frequency  $f$ , and  $T_{cp}$  is counted as  $n_2$  by the clock frequency  $f_c$ :

$$n_2 = 2\pi f_c R_R n_1 C_p.$$

The clock frequency is selected so that  $C_p$  is directly obtained.

Next, step 6 immediately initiates the D measurement. Switch  $S_D$  is connected to  $e_1$  and the phase of the detector signal is controlled at  $0^\circ$ . The phase-detected dc voltage is integrated and discharged in steps 6 and 7, with the phase of the detector signal changed from  $0^\circ$  to  $270^\circ$  in step 7. If the discharge time is  $T_d$ ,

$$Q_{d1} = -K G_p R_R T_2 e_2 \quad \text{in step 6, and}$$

$$Q_{d2} = K \omega C_p R_R T_d e_2 \quad \text{in step 7.}$$

If the charging time is  $n'_2$  times the period of the clock frequency, the following equation is similarly established:

$$\frac{n'_2}{f_c} K \omega C_p R_R e_2 = \frac{n'_1}{f_c} K G_p R_R e_2$$

$$n'_2 = n'_1 \frac{G_p}{\omega C_p} = n'_1 D$$

Thus  $n'_2$  is a measure of the dissipation factor.

### $C_s$ -D Measurement

The  $C_s$ -D measurement employs an unusual technique.  $e_1$  is the reference signal for the series equivalent circuit mode. In step 3,  $S_D$  is connected to  $e_1$  and phase detected by a signal in phase with  $e_1$ . In other words,  $e_1$  is phase detected by  $e_1$ . The integrator is charged for a period equal to  $n_3$  times the reciprocal of the test frequency  $f$ . The charge stored on the integrator during this time is:

$$Q_{cs1} = K e_1 n_3 / f.$$

Step 4 is the discharge cycle.  $S_D$  is connected to  $e_2$ , which is phase detected by a signal whose phase is shifted from  $e_1$  by  $270^\circ$ . The integrator discharges until its output crosses the zero-volt point. If the discharge time is  $n_4/f_c$ , the charge dissipated is:

$$Q_{cs2} = -K \frac{1}{\omega C_s R_R} \frac{n_4}{f_c} e_1$$

Then, because

$$Q_{cs1} = -Q_{cs2},$$

$$n_4 = 2\pi f_c n_3 C_s R_R.$$

Hence from  $n_4$ ,  $C_s$  is directly obtained.

This technique is the widely used dual-slope method except that the slopes occur in reverse order. Usually, the integrator discharge slope is constant, but here the slope decreases as the C count increases. At full scale, the discharge slope is one-tenth that of the charging slope. This results in a good signal-to-noise ratio and precise resolution, and makes it possible for the new meter to use only five range resistors for its eight-range measurement capability.



#### Four-Phase Generator

The precision 90° phase shift needed for phase detection is normally derived from a standard capacitor, but when the test frequency is low, such as 120 Hz, standard capacitors are very expensive and very large. The 4261A measures L, C, R, and D without a standard capacitor. The four-phase generator technique makes this possible.

Fig. 5 is a circuit diagram of the four-phase generator. The reference signal is shaped and fed to a phase detector (point A) whose other input is the 0° output signal, thus forming a phase-locked loop. The filtered phase detector output tunes a voltage controlled oscillator that produces a signal at four times the input frequency. Two J-K flip flops driven by the VCO provide 0°, 90°, 180° and 270° four-phase outputs.

A potential problem of this method is phase noise, which causes fluctuations in counting the discharge time. In the 4261A phase noise is less than -70 dB.

#### Sectional Average Integrator

The phase-detected signal of Fig. 3 has to be translated into a dc voltage very quickly for precise operation of the dual-slope technique. The sectional average integrator<sup>1</sup>, or SAI, (Fig. 6) is especially useful at the 120 Hz test frequency. If  $C_i R_f$  is suitably selected the settling time is one test signal period.

During the first period  $T$ , the input current is integrated by the integrator. At the end of this period, the integrator output  $E_1$  is proportional to the dc input current. After the first period,  $E_1$  is transferred to  $C_1$  by momentarily closing switch  $S_h$ . Thus the output  $E_0$  is a step function whose steady-state value is exactly proportional to  $I_{DC}$ . Fig. 6 shows typical waveforms.

#### Auto Phase Adjust

A phase error compensation technique was first employed in the 4271A 1 MHz Digital LCR Meter.<sup>2</sup> That method used two phase detectors and two integrators. To produce a quality low-cost unit, an auto phase adjustment technique was adopted for the 4261A. The auto phase adjustment block diagram is

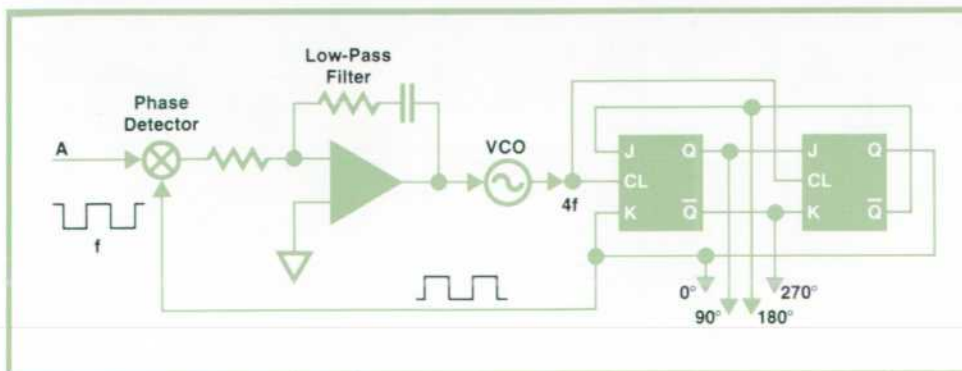


Fig. 5. Four-phase generator develops precision phase shifts and eliminates the need for a standard capacitor.

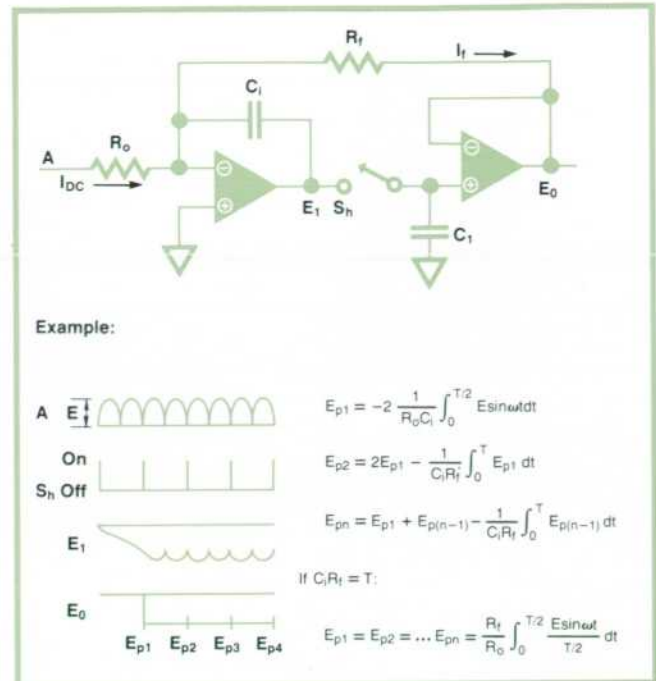


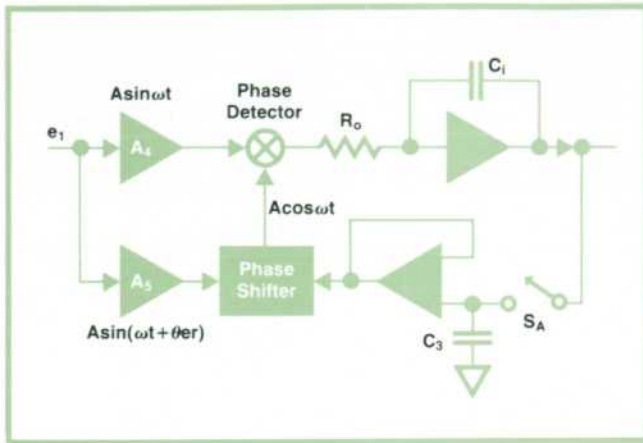
Fig. 6. Sectional average integrator converts the phase-detected signal to a dc voltage within one test signal period, as shown by the typical waveforms.

shown in Fig. 7. Amplifiers  $A_4$  and  $A_5$  in Fig. 7 are the same as those in Fig. 3. Since the amplifiers are not ideal, they shift the phase of the  $e_1$  and  $e_2$  signals. The difference between the two phase shifts ( $\theta_{er}$ ) will cause a large error, especially when measuring the dissipation factor of low-loss capacitors. For accuracy,  $\tan \theta_{er}$  must be less than 0.001.

Automatic phase adjustment is done in step 2 of the measurement sequence.  $S_A$  is closed and a first-order feedback loop is created through the integrator to reduce  $\theta_{er}$ . When the loop has settled, a dc voltage proportional to  $\theta_{er}$  is stored in  $C_3$  and maintained for the measurement period.

#### ROM-Centered Design

To control its various measurement modes and to manage the complex decoding necessary to provide simple operation with wide-range measurements, the



**Fig. 7.** Circuit diagram for auto phase adjustment. Closing  $S_A$  creates a first-order feedback loop that stores on capacitor  $C_3$  a voltage proportional to the differential phase shift of amplifiers  $A_4$  and  $A_5$ .

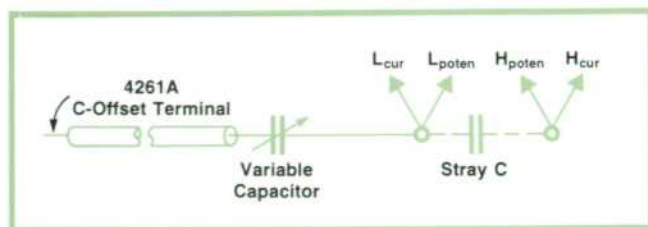
4261A uses a ROM-centered design. It has two 4K-bit ROMs, one for sequence control and the other a decoder. With this design, it was easy to add the self-test functions. The ROMs are n-channel MOS ROMs manufactured by HP.

#### Full Autoranging

The 4261A has two autoranging modes. One is a fixed measurement circuit mode in which the operator selects either the series or the parallel equivalent circuit, and the other is full autoranging including circuit mode changing. Measurement circuit mode changes are done by switching  $S_C$  in Fig. 3. In the full autoranging mode, the instrument selects an appropriate range from the eight available ranges according to the value of the component being tested. In this mode, the function switch need only be set to L, C, or R to make the measurement.

#### Self-Test

The 4261A has self-test functions that enable it to check most performance areas. No additional equipment or circuitry is required for making the self-check.



**Fig. 8.** To cancel stray capacitance between the unknown terminals, a capacitance offset signal, available at a rear-panel connector, provides a capacitance offset of 0 to 100 pF when fed into the low-current terminal through a variable capacitor. The capacitor is adjusted for a zero display with no unknown connected.

The user need only set two slide switches. Two tests are provided. One tests the logic systems and the other mainly checks the analog circuits. Slide switches located on the sequence control board are set to the appropriate positions to put the 4261A into its self-test mode.

#### Minimizing Errors

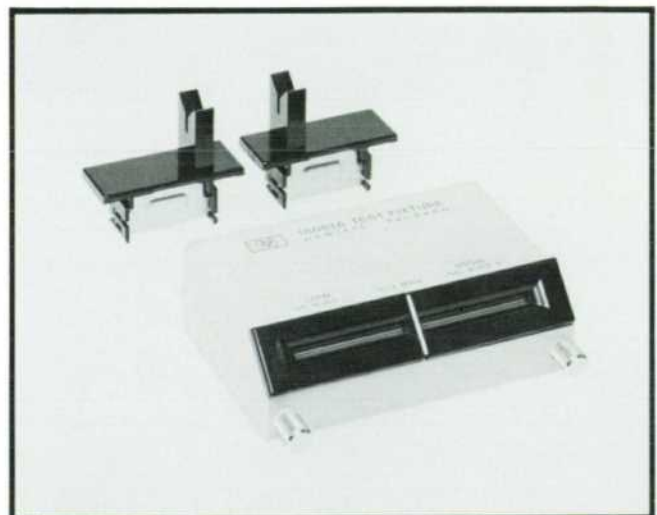
The five-terminal connection configuration minimizes the measurement error caused by residual impedance of the test leads. It is especially useful for the measurement of low impedances (below 1Ω). However, some care is required in making the test lead connections when measuring capacitors from 100 to 1000 μF at 1 kHz. Here, an error is caused by the mutual inductance of the Hp, Hc cable or the Lp, Lc cable. If the mutual inductance of each cable is M/2 henries, then:

$$C_{\text{measured}} = \frac{C_x}{1 - \omega^2 M C_x}$$

To minimize this error, it is necessary to use short test leads or to twist the Hp and Lp cables together. Similarly in high-impedance measurements, it is possible to minimize the stray capacitance between the high and low terminals by shielding with the GUARD terminal. Compensation for high-impedance measurement errors can also be made by using an offset voltage equal to the voltage across the DUT but opposite in polarity; this is done with the 4261A in the connection configuration shown in Fig. 8. The variable capacitor is adjusted for a zero display.

#### Accessories

Several accessories are available for the 4261A. The 16061A Test Fixture is a direct-connection type for



**Fig. 9.** Model 16061A Test Fixture for general-purpose use.



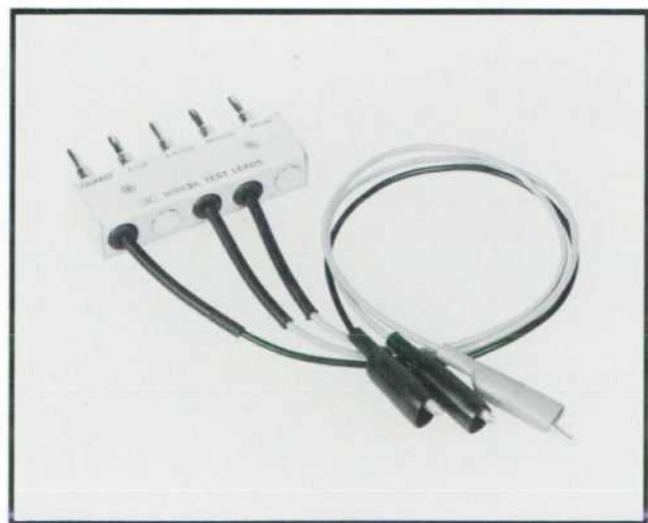


**Fig. 10.** Model 16062A Test Leads for low-impedance devices.

general-purpose use. The 16061A Test Fixture (Fig. 9) has inserts for both parallel and axial lead components. The 16062A Test Leads (Fig. 10) are for comparatively low-impedance DUTs (four-terminal connections). The 16063A Test Leads (Fig. 11) are for comparatively high-impedance DUTs (three-terminal connections).

#### Acknowledgments

The authors wish to express appreciation to the many people who participated in the development of the Model 4261A. The team members included Kohichi Maeda, who directed the project, Hiroshi Sakayori, who designed the process amplifier section, Kenzo Ishiguro, who designed the display and decoder section, Seiji Mochizuki, who did the power supply design, Toshio Manabe and Yoshimasa Shibata, who contributed to the mechanical design, and



**Fig. 11.** Model 16063A Test Leads for high-impedance devices.

Kazu Shibata and Yoshio Satoh, who handled the industrial design. Hitoshi Noguchi provided many useful suggestions for the project. Akira Yamaguchi designed part of the logic section in the early stages of the project.

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1. T. Sugiyama and K. Yamaguchi, "Pulsewidth Modulation DC Potentiometer," IEEE Transactions, Vol. IM-19, No. 4, November 1970.
2. K. Maeda, "An Automatic Precision, 1-MHz Digital LCR Meter," Hewlett-Packard Journal, March 1974.

#### Satoru Hashimoto



Satoru Hashimoto received his BSEE from Tokyo Metropolitan University in 1971, and soon afterwards joined Yokogawa-Hewlett-Packard. He worked on the design of the logic section of the 4271A 1-MHz Digital LCR Meter, then joined the 4261A Digital LCR Meter project. He developed the counter and the sequence control section circuitry for the 4261A. In his spare time Satoru enjoys mountain climbing and photography.

#### Toshio Tamamura



Toshio Tamamura received his BSEE degree in 1971 from the University of Electro-Communications in Tokyo. He has been with Yokogawa-Hewlett-Packard as a development engineer since that time. He was a principal contributor to the design of the 4271A 1-MHz Digital LCR Meter and the 4261A Digital LCR Meter; he developed the analog section circuitry for the 4261A. He's married and the father of a small son. In his spare time Toshio likes to play tennis.

## SPECIFICATIONS

### HP Model 4261A LCR Meter

#### Common Specifications

**PARAMETERS MEASURED:** C-D, L-D, R  
**DISPLAY:** 3½ digit, max. display 1900  
**CIRCUIT MODES:** auto, parallel and series  
**MEASUREMENT CIRCUIT:** five-terminal method  
**RANGE MODE:** auto or range hold  
**MEASUREMENT FREQUENCIES:** 120 Hz  $\pm 3\%$  and 1 kHz  $\pm 3\%$   
**TRIGGER:** internal, manual, or external

#### C-D Measurement

Range	120 Hz 1 kHz	1000 pF 1000 pF	10.00 nF 10.00 nF	100.0 nF 100.0 nF	1000 nF 1000 nF	10.00 $\mu$ F 10.00 $\mu$ F	100.0 $\mu$ F 100.0 $\mu$ F	1000 $\mu$ F 1000 $\mu$ F
Test Signal Level	Parallel	1V or 50 mV						
(Note 1)	Series				10 $\mu$ A	100 $\mu$ A	1 mA	10 mA
	Auto	Same as parallel mode			Same as series mode			
C Accuracy	Parallel	0.2% + 1 count + 0.2 pF			Test signal = 1V			
	Series	0.5% + 3 counts			Test signal = 50 mV			
	Auto	0.3% + 2 counts			0.5% + 2 counts			
(Note 2)	Auto	Same as parallel mode			Same as series mode			
D Accuracy	Parallel	0.2% + (2 + 200/Cx) counts			Test signal = 1V			
	Series	0.3% + (2 + 1000/Cx) counts			Test signal = 50 mV			
	Auto	0.3% + (2 + Cx/500) counts			1% + (5 + Cx/500) counts			
(Note 2)	Auto	Same as parallel mode			Same as series mode			

1. Typical data. Varies with value of D and number of counts.
  2.  $\pm$  (% of reading + counts +  $\alpha$ ). Cx is capacitance readout in counts.
  3. (5% + 2 counts) at 1 kHz.
- Accuracy applies over a temperature range of 23°C  $\pm$  5°C. Error doubles for 0-55°C.

#### L-D Measurement

Range	120 Hz 1 kHz	1000 $\mu$ H 100.0 $\mu$ H	10.00 mH 10.00 mH	100.0 mH 100.0 mH	1000 mH 1000 mH	10.00 H 10.00 H	100.0 H 100.0 H
Test Signal Level	Parallel	1V					
(Note 1)	Series	70 mA	10 mA	1 mA	100 $\mu$ A	10 $\mu$ A	
	Auto	Same as series mode			Same as parallel mode		
L Accuracy	Parallel	0.3% + 2 counts			1% + 2 counts		
	Series	0.2% + 2 counts + 0.2 $\mu$ H					
	Auto	Same as series mode			Same as parallel mode		
(Note 2)	Auto	Same as series mode			Same as parallel mode		
D Accuracy	Parallel	0.3% + (3 + Lx/500) counts			1% + (3 + Lx/500) counts		
	Series	0.2% + (3 + 200/Lx) counts					
	Auto	Same as series mode			Same as parallel mode		
(Note 2)	Auto	Same as series mode			Same as parallel mode		

1. Typical data. Varies with value of D and number of counts.
  2.  $\pm$  (% of reading + counts +  $\alpha$ ). Lx is inductance readout in counts.
- Accuracy applies over a temperature range of 23°C  $\pm$  5°C. Error doubles for 0-55°C.

#### R Measurement

Range	120 Hz 1 kHz	1000 mΩ	10.00Ω	100.0Ω	1000Ω	10.00 kΩ	100.0 kΩ	1000 kΩ	10.00 MΩ	
Test	Parallel	1V								
Signal	Series	70 mA	10 mA	1 mA	100 μA	10 μA				
(Note 1)	Auto	Same as series mode				Same as parallel mode				
R	Parallel					0.3% + 2 counts				
Accuracy	Series	0.2% + 2 counts								
	Auto	Same as series mode				Same as parallel mode				
	(Note 2)	Auto				Same as parallel mode				

1. Typical data. Varies with number of counts.
  2.  $\pm$  (% of reading + counts).
- Accuracy applies over a temperature range of 23°C  $\pm$  5°C. Error doubles for 0-55°C.

#### DC Bias

**INTERNAL SOURCE:** 1.5V, 2.2V, 6V (selectable on front panel). Accuracy  $\pm 5\%$ .  
**EXTERNAL SOURCE:** Provision for external dc bias voltage of +30V maximum at binding posts on rear panel.

#### General

**OPERATING TEMPERATURE AND HUMIDITY:** 0° C to 55°C, to 95% RH at 40°C.  
**VOLTAGE REQUIREMENTS:** 100/120/220/240  $\pm$  10% 48-66 Hz  
**POWER CONSUMPTION:**  $\leq 25$  W with any option.  
**DIMENSIONS:** 213 W  $\times$  134 H  $\times$  422 D mm  
**WEIGHT:** Approximately 6 kg

#### Reference Data

**MEASURING TIME:** the period between start of a measurement and completion of the measurement is equal to measuring time when RANGE HOLD is set to ON plus time required for autoranging. The following are typical times for a measurement of approximately 1000 counts on low loss components when RANGE HOLD is set to ON.

1 kHz: C/L, 220-260 ms; R, 120-160 ms

120 Hz: C/L, 900 ms; R, 700 ms

**TIME REQUIRED FOR AUTORANGING (RANGE HOLD OFF):**

1 kHz: 180  $\times$  n ms

120 Hz: 670  $\times$  n ms

where n is the number of ranges stepped by the autorange circuit.

**READING RATE:** the period between the start of a measurement and the start of the next measurement is equal to the measuring time plus 30 milliseconds (typical) hold time.

**PRICE IN U.S.A.:** \$1740.

**MANUFACTURING DIVISION:** YOKOGAWA HEWLETT-PACKARD, LTD.

9-1, Takakura-cho  
Hachioji-shi  
Tokyo 192 Japan

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

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